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ATX
Ver: 1.0

Intel -Coffeelake plamform Z370

CPU:

coffeelake-S

System Chipset:

Z370

Onboard Chip:

HD Audio Codec:ALC892

LAN:INTEL I219

SIO:Nuvoton 6795

Flash ROM: SPI 128MB

Main Memory:

DDRIV (2133MHz/2400MHz) * 4 (Dual Channel)

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

PCI Express (X16) Slot *1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 4
M2 * 2

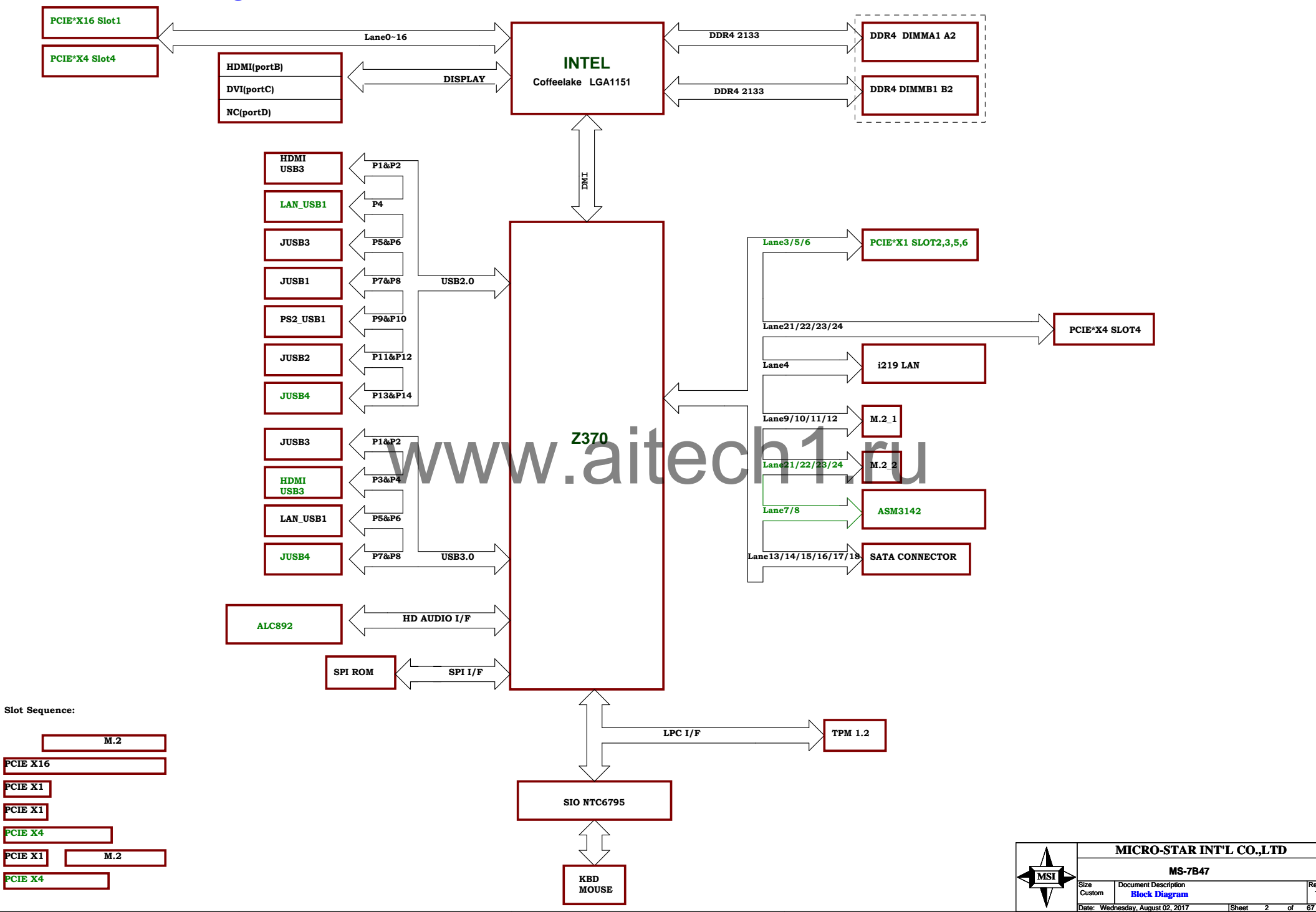
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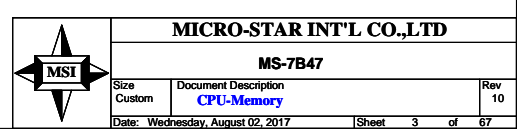
SATA3.0 x6 (PCH)
FRONT USB2.0 *4
FRONTUSB3.0 *4
REAR USB3.0 *4
REAR USB2.0 *2
REAR USB TYPE A+C

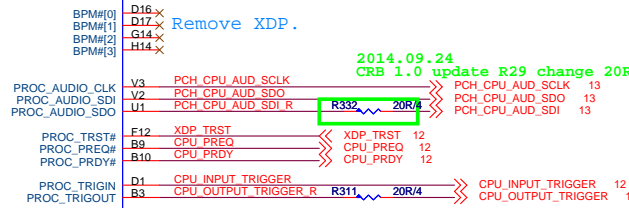
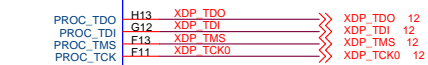
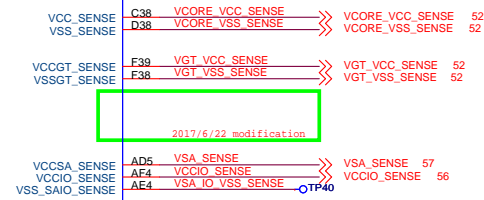
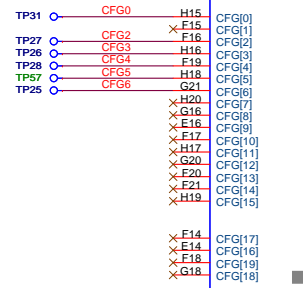
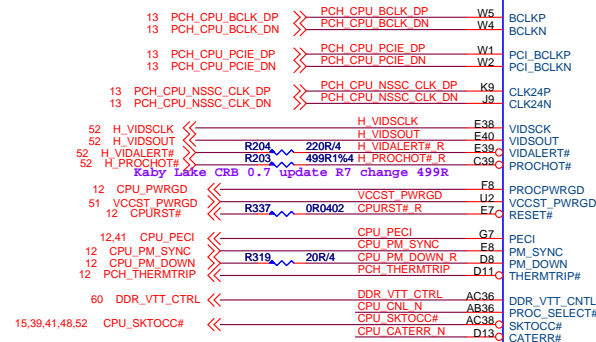
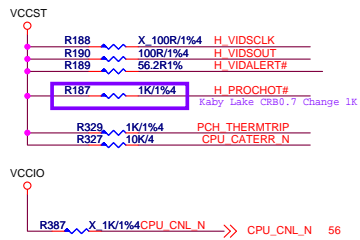


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MS-7A68 Block Diagram



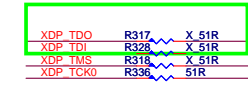




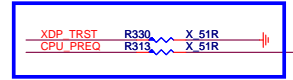
CFG Strap

CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

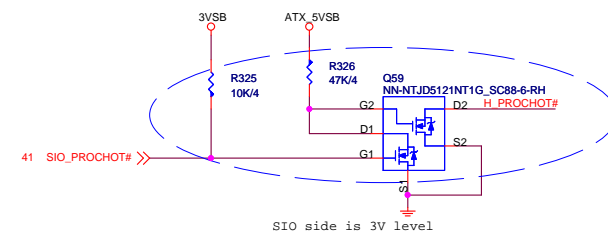
2014.09.29 remove



Close CPU <1100 mil
1000 mil < CPU_XDP_MBP0~1 < 6000 mil



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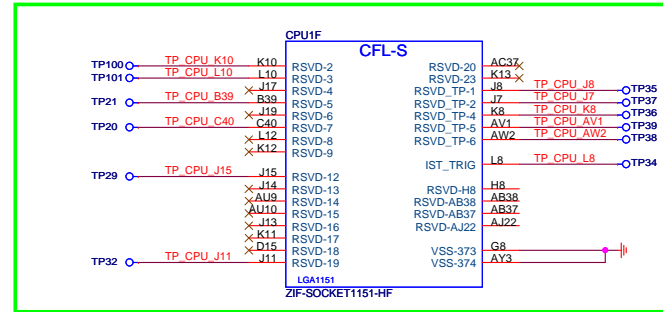
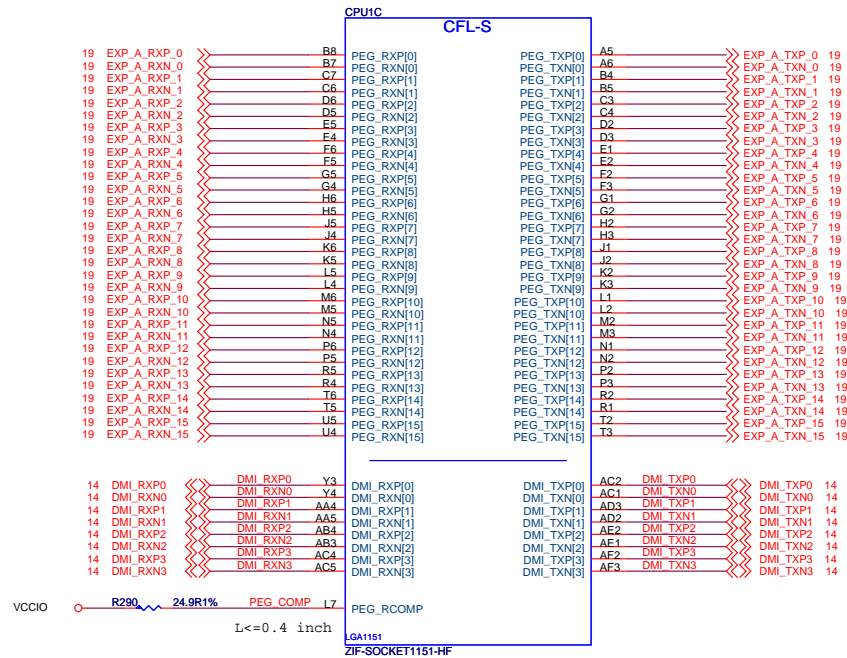


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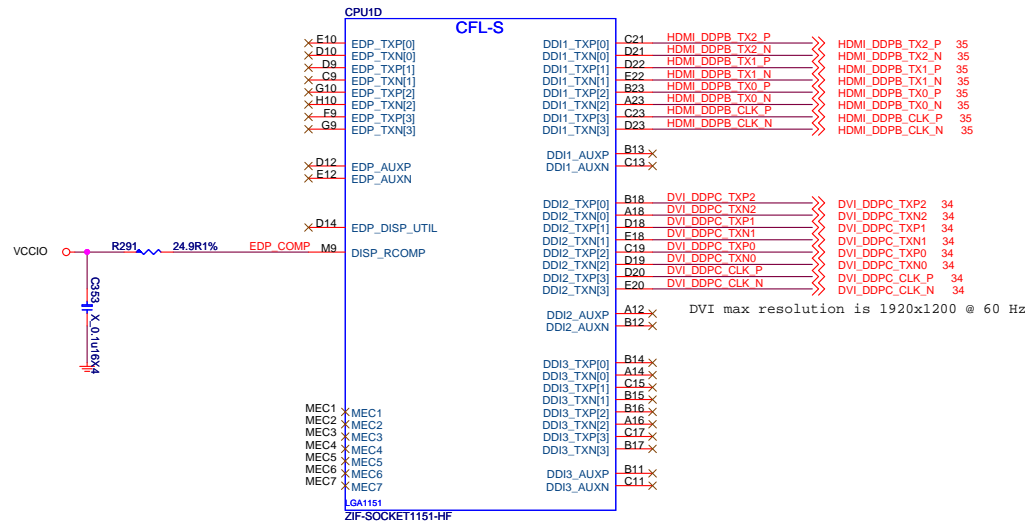
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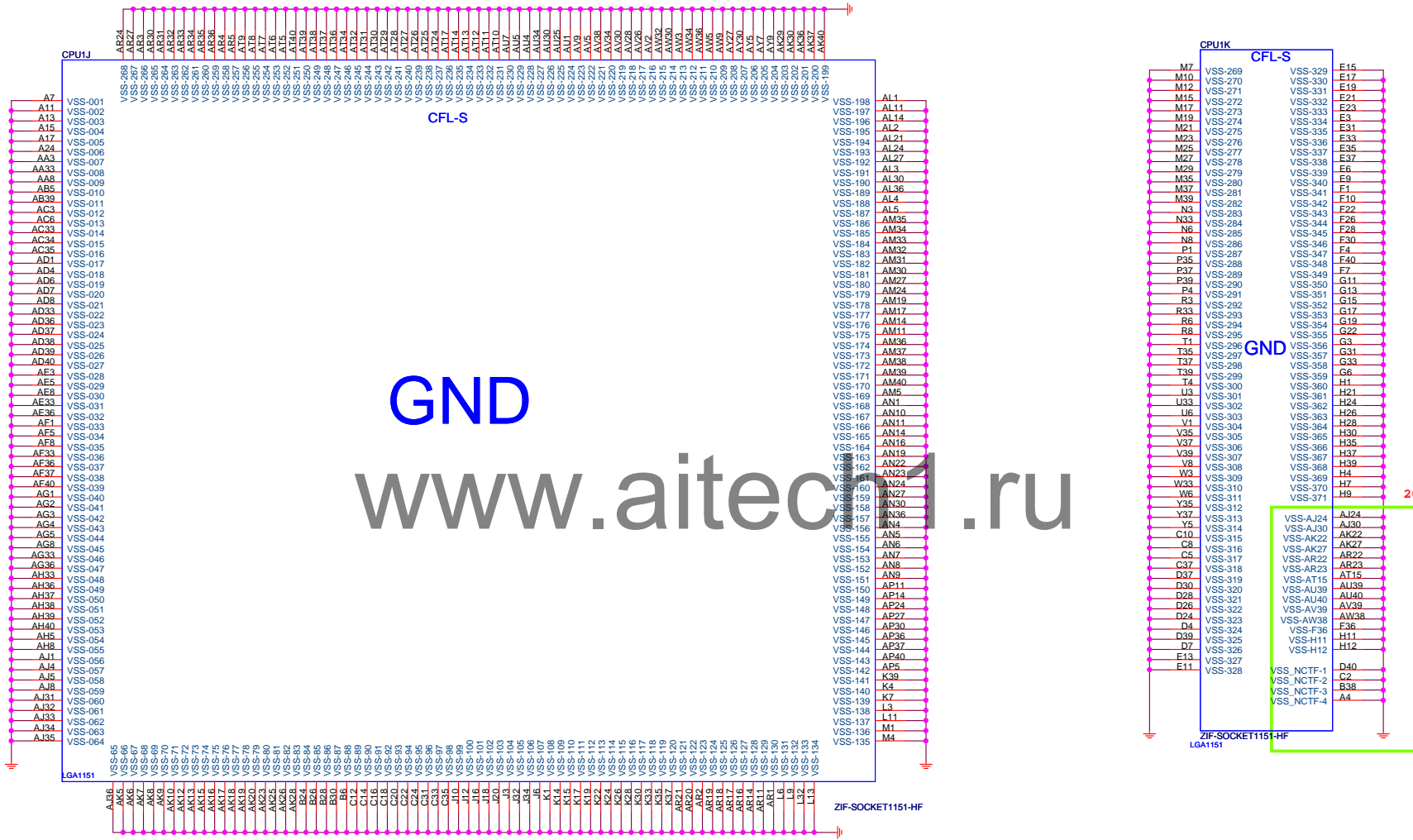
2017/6/22 modification

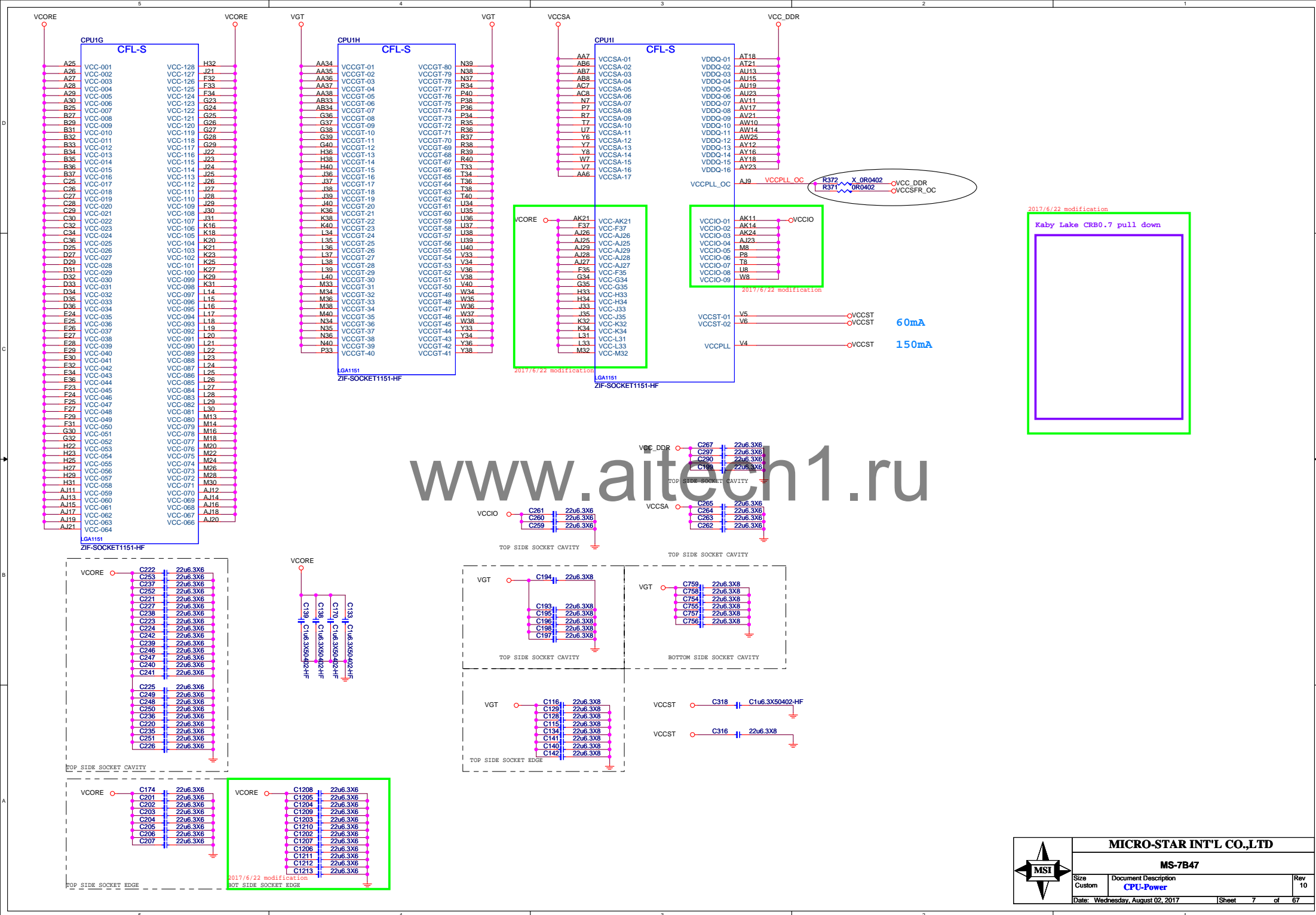


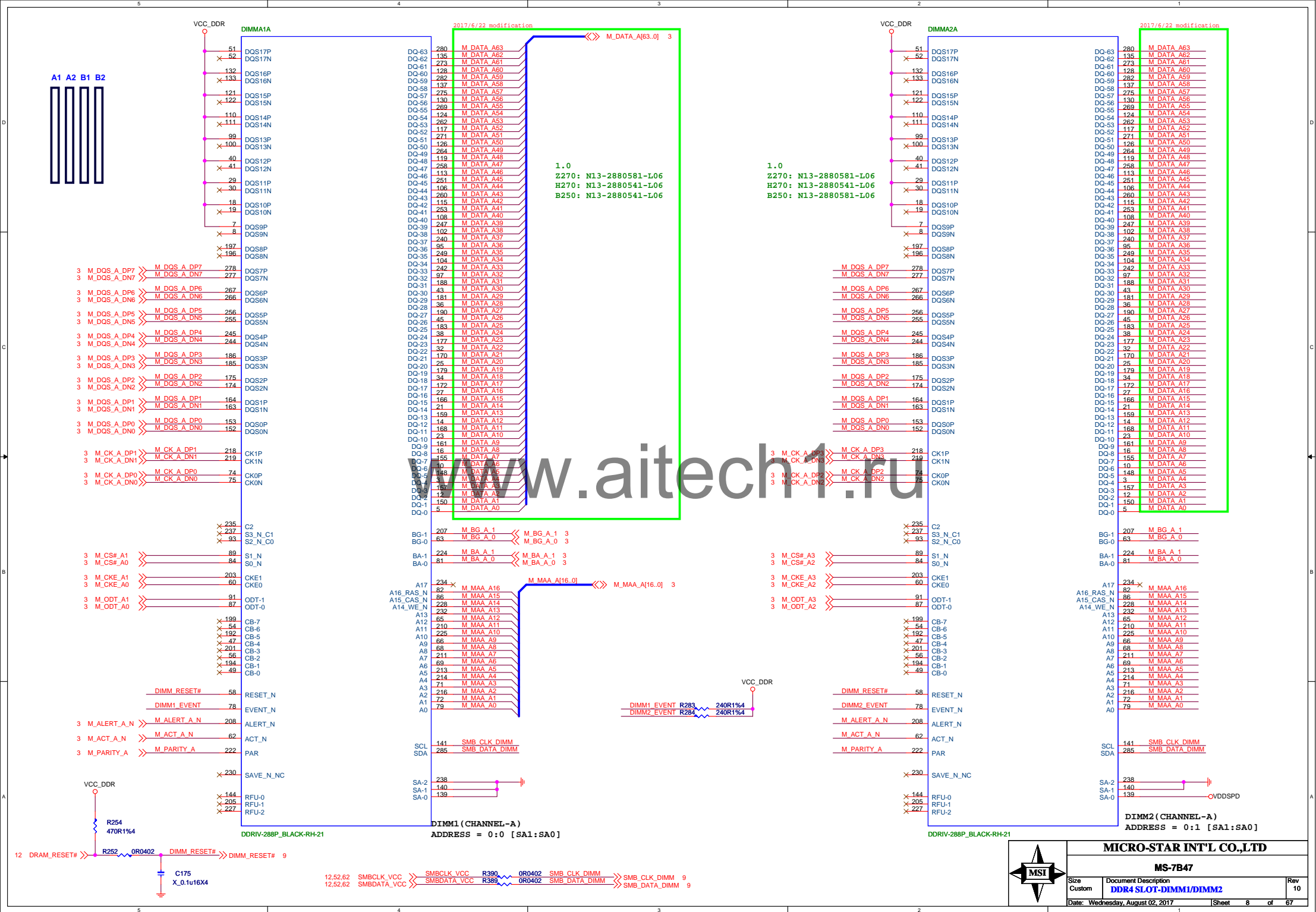
TP35, TP37, TP36, TP39, TP38, TP34, TP100, TP101
Reservd for CPU XDP debug pin

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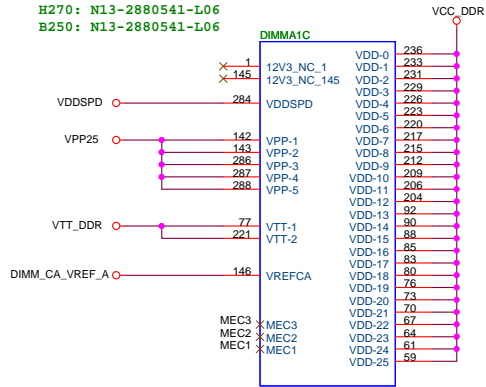




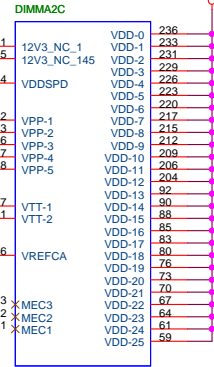
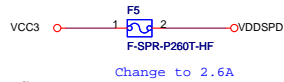
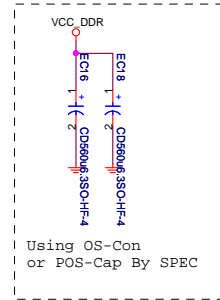




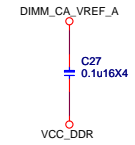
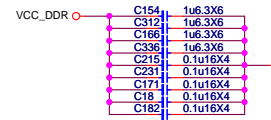
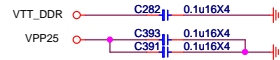
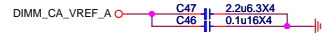
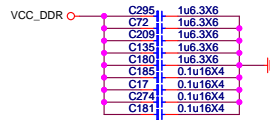
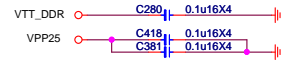
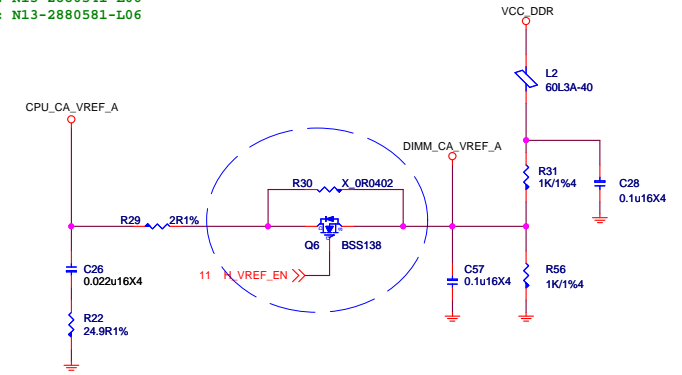
1.0
Z270: N13-2880581-L06
H270: N13-2880541-L06
B250: N13-2880541-L06



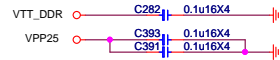
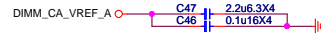
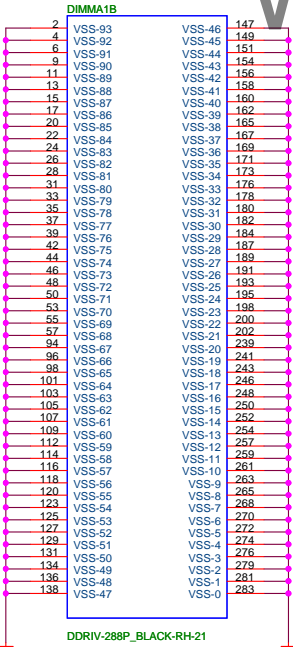
DIMM SLOT PN BY SPEC



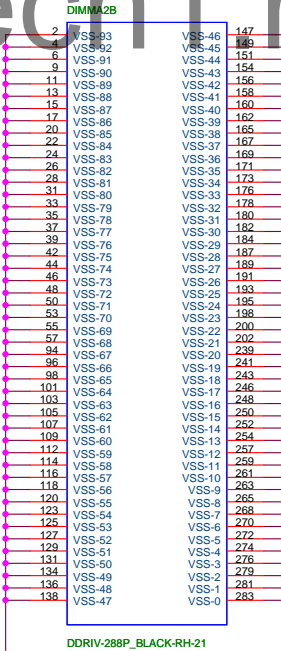
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Z270: N13-2880581-L06
H270: N13-2880541-L06
B250: N13-2880581-L06



1.0
Z270: N13-2880581-L06
H270: N13-2880541-L06
B250: N13-2880541-L06



1.0
Z270: N13-2880581-L06
H270: N13-2880541-L06
B250: N13-2880581-L06

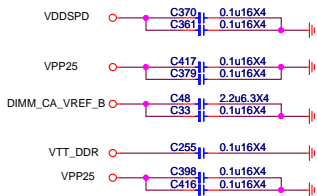
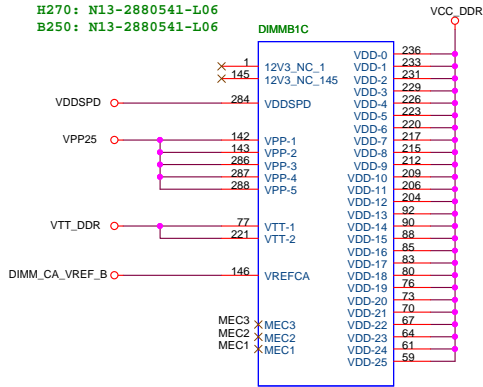


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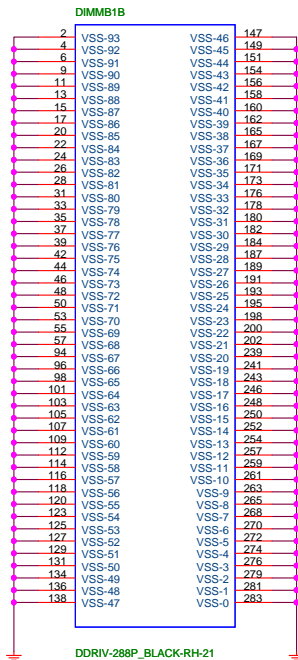
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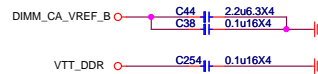
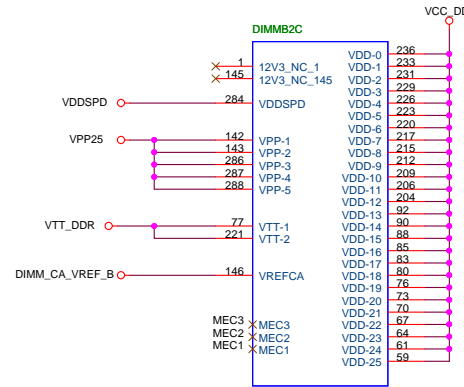
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Z270: N13-2880581-L06
H270: N13-2880541-L06
B250: N13-2880541-L06



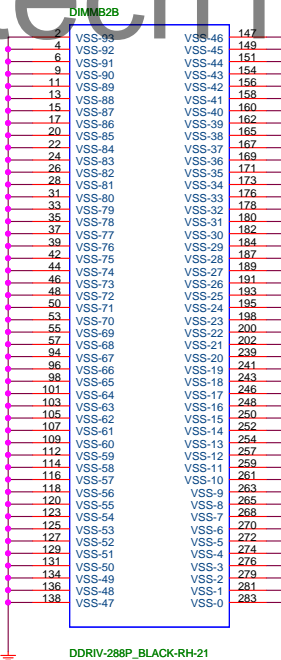
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Z270: N13-2880581-L06
H270: N13-2880541-L06
B250: N13-2880541-L06



DDRIV-288P_BLACK-RH-21

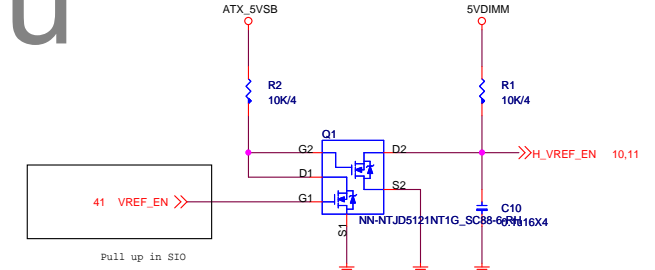
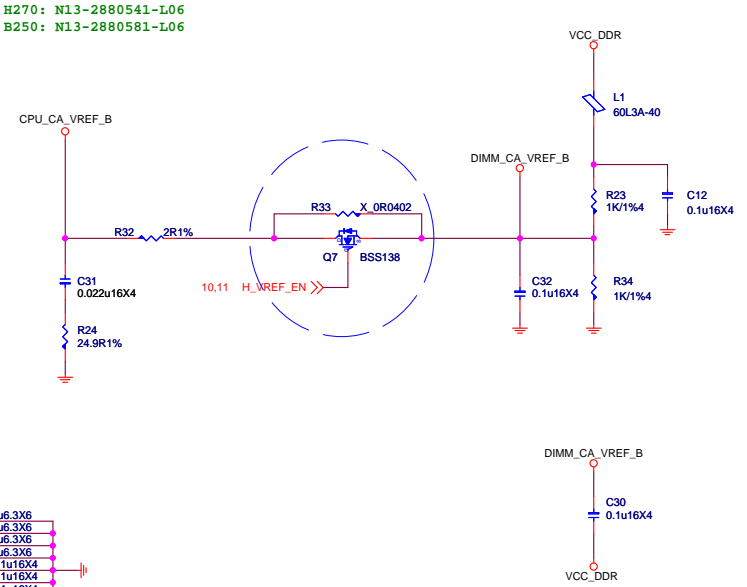


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B250: N13-2880581-L06



DDRIV-288P_BLACK-RH-21

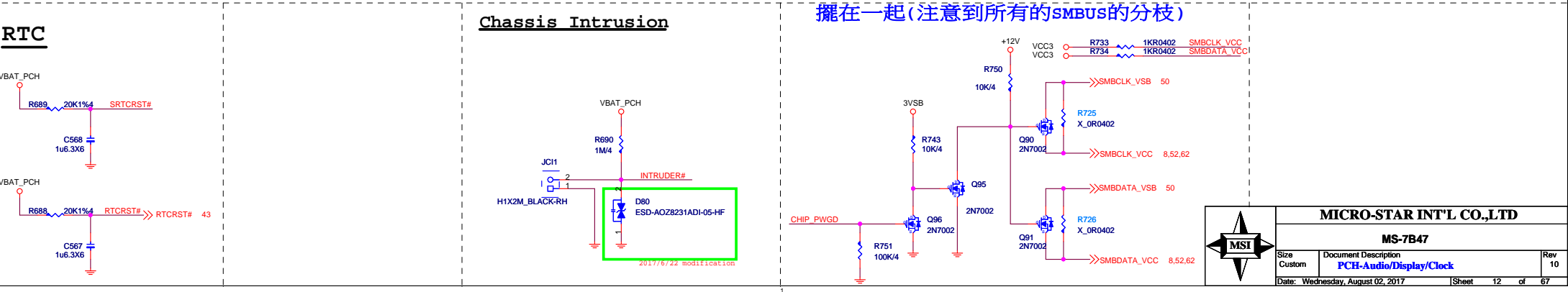
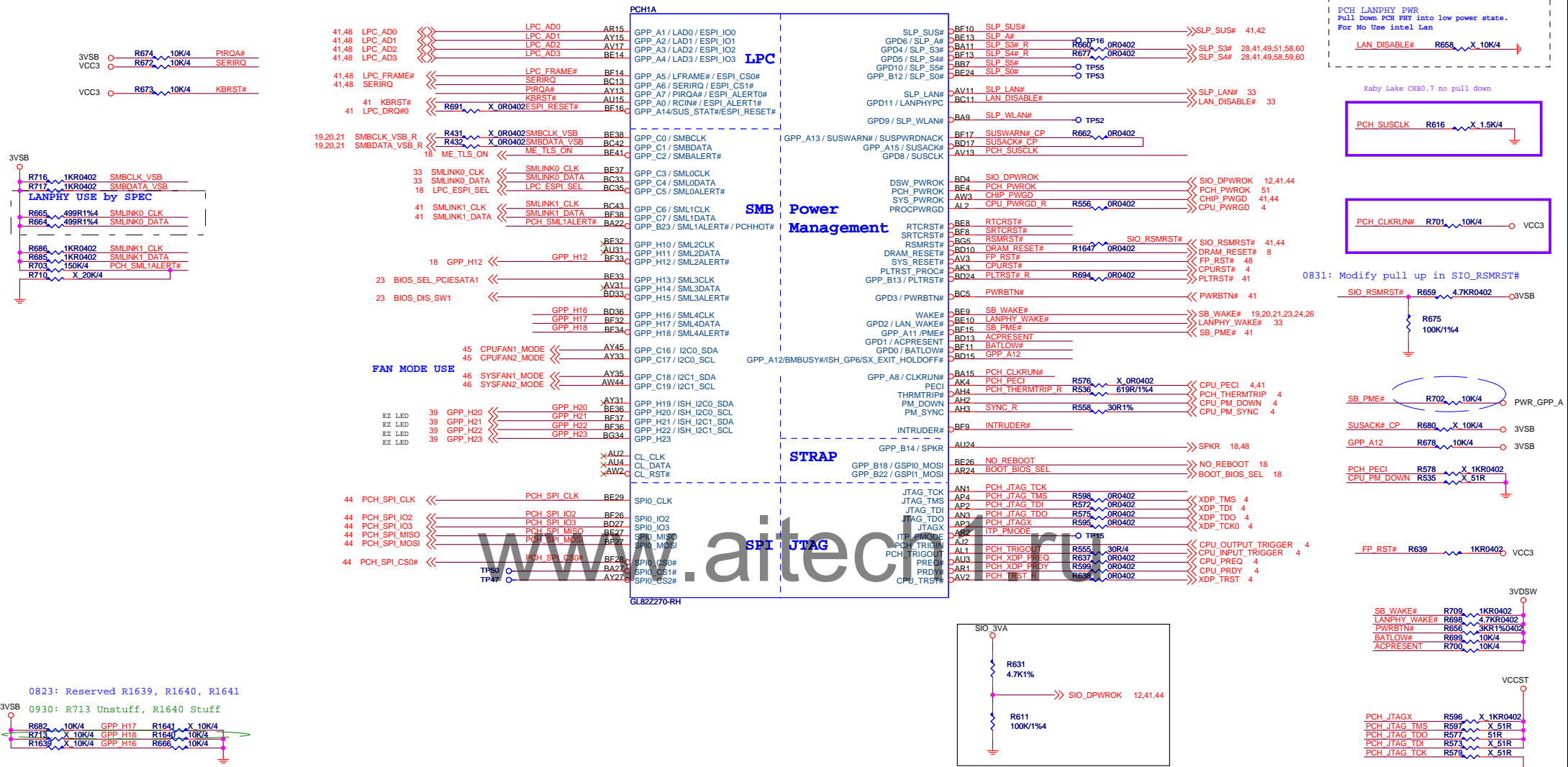
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H270: N13-2880541-L06
B250: N13-2880581-L06



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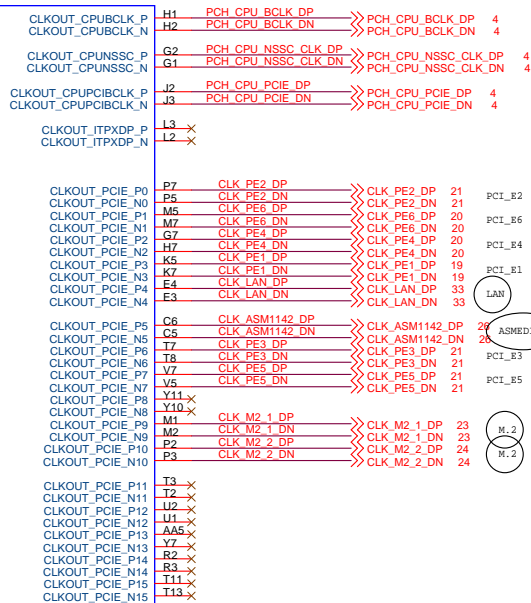
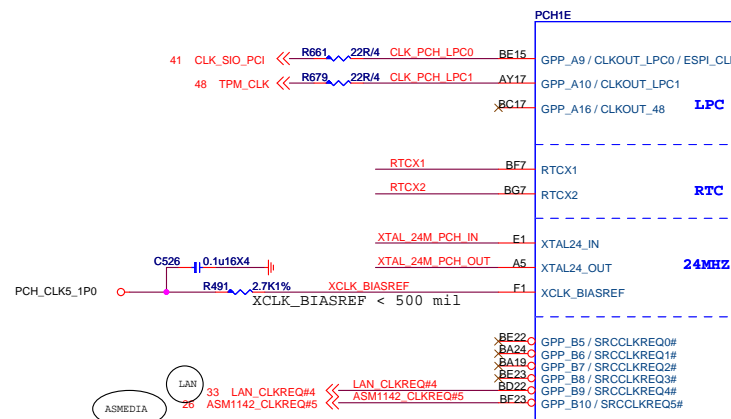
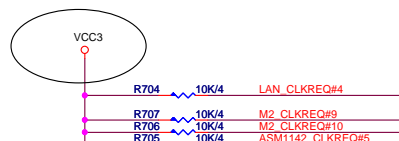
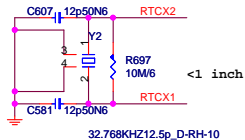
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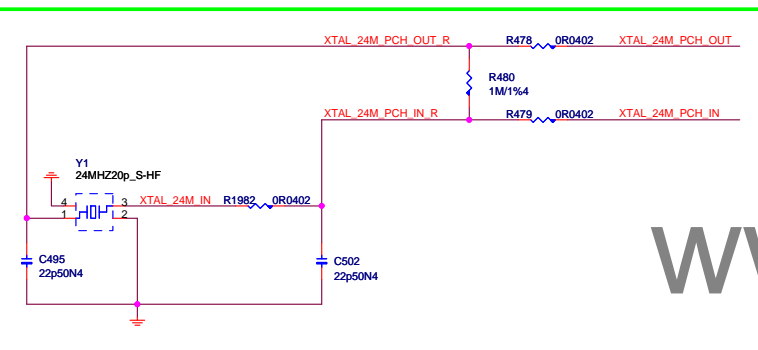
PCH_CLK

RTC Block

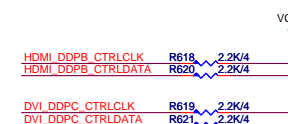
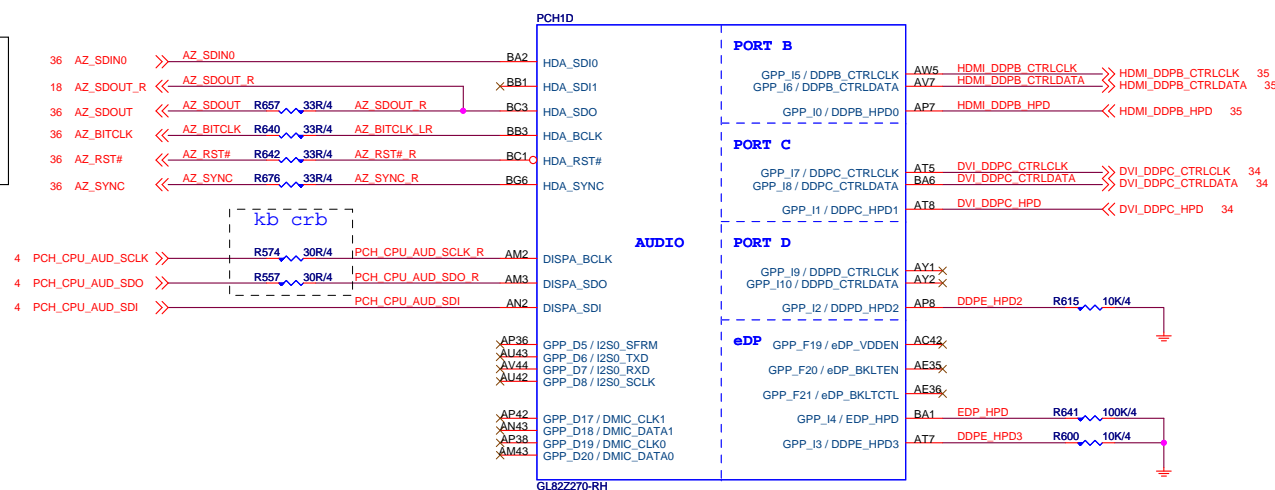
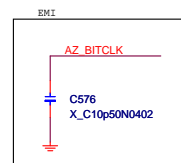
Close to PCH



2017/6/22 modification



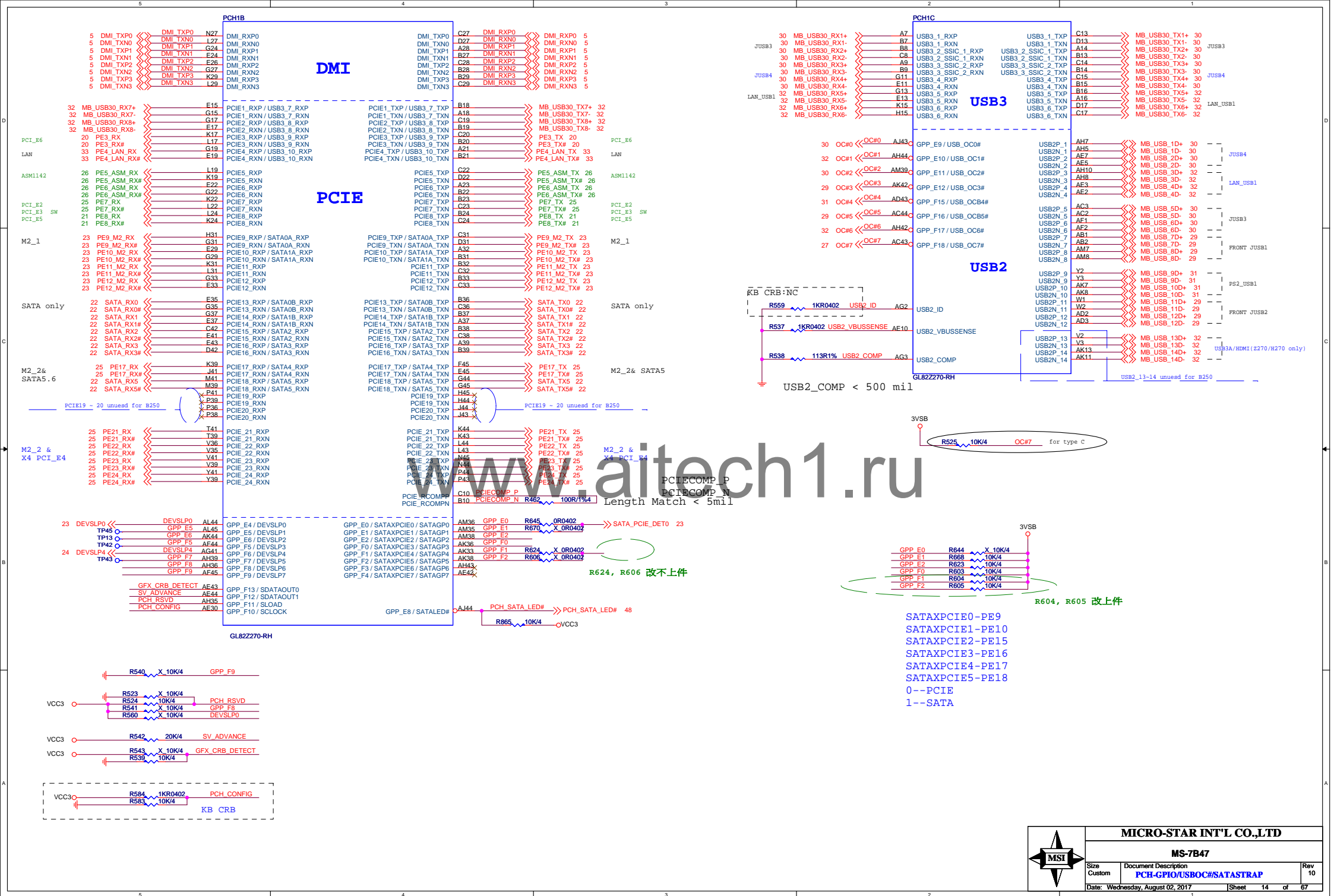
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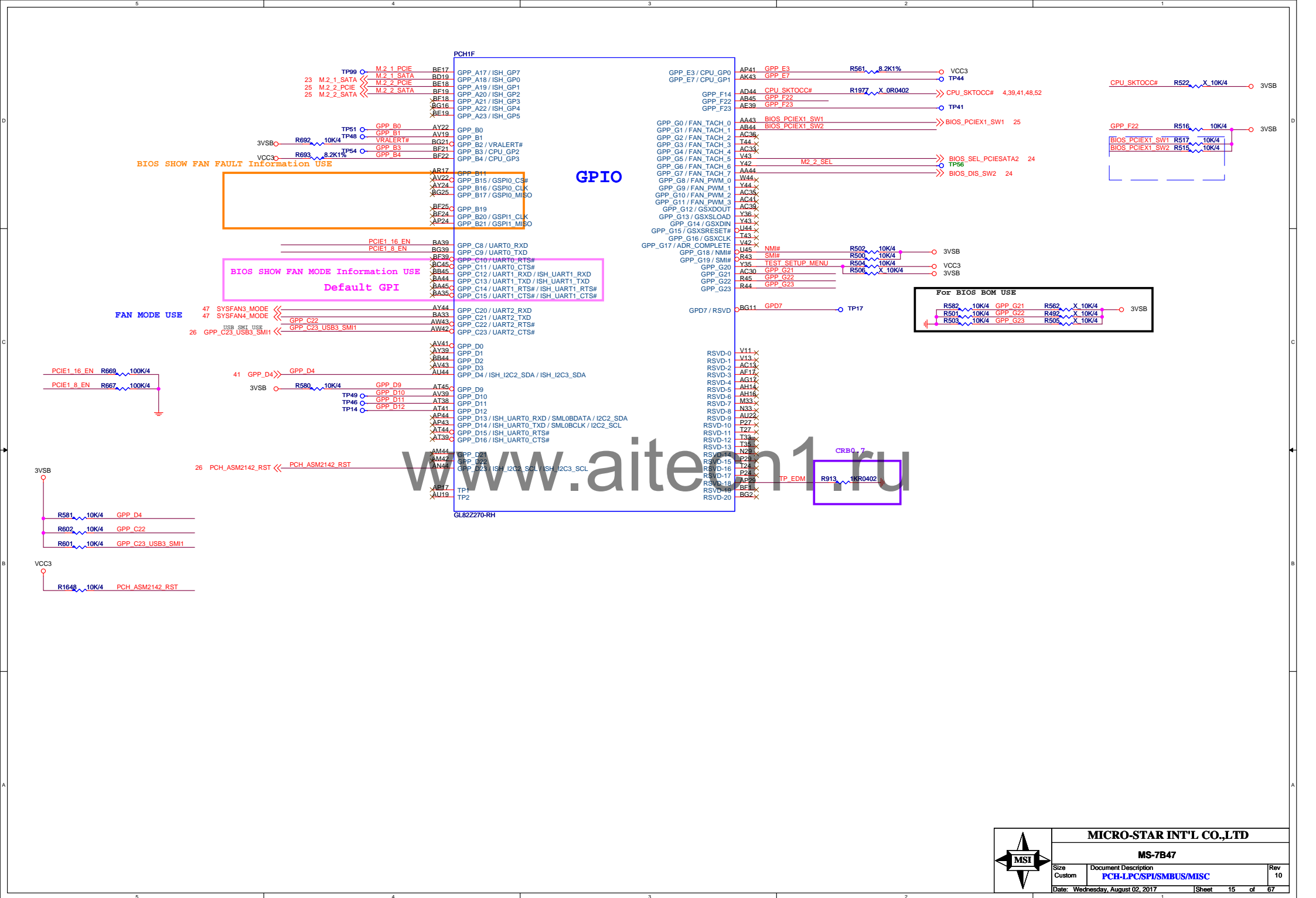


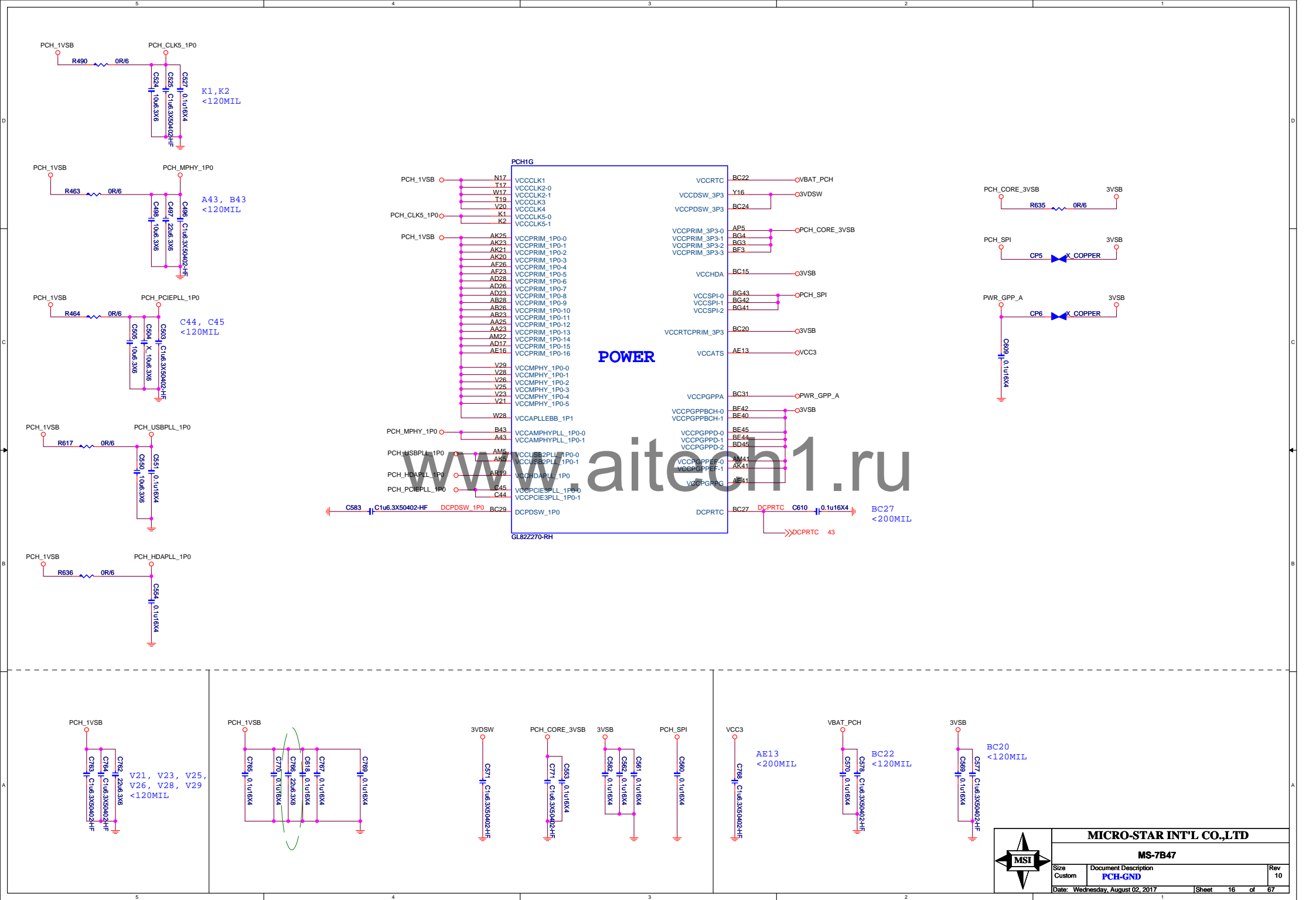
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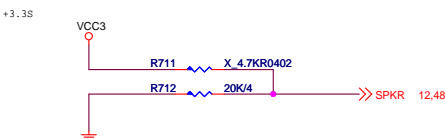




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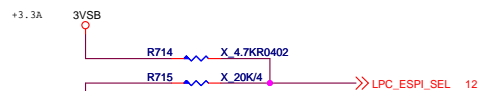


TOP Swap



Internal pull-down is disabled after PLTRST#

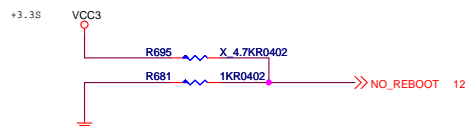
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

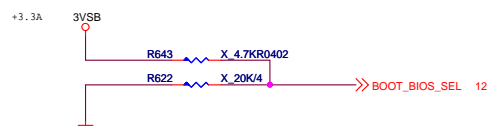
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

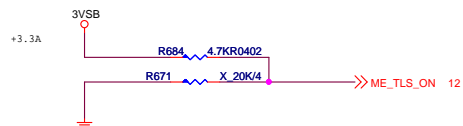
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

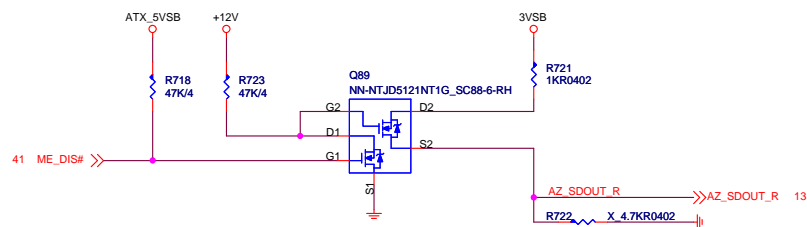
AMT and SBA with confidentiality



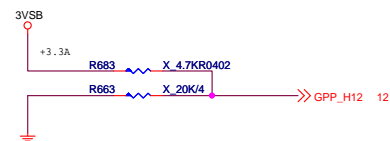
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



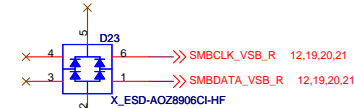
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

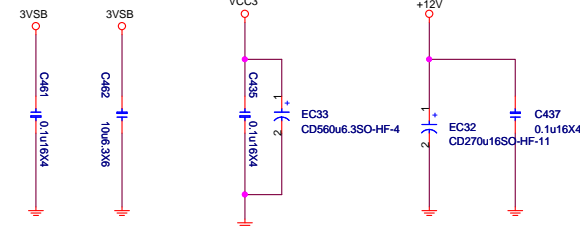
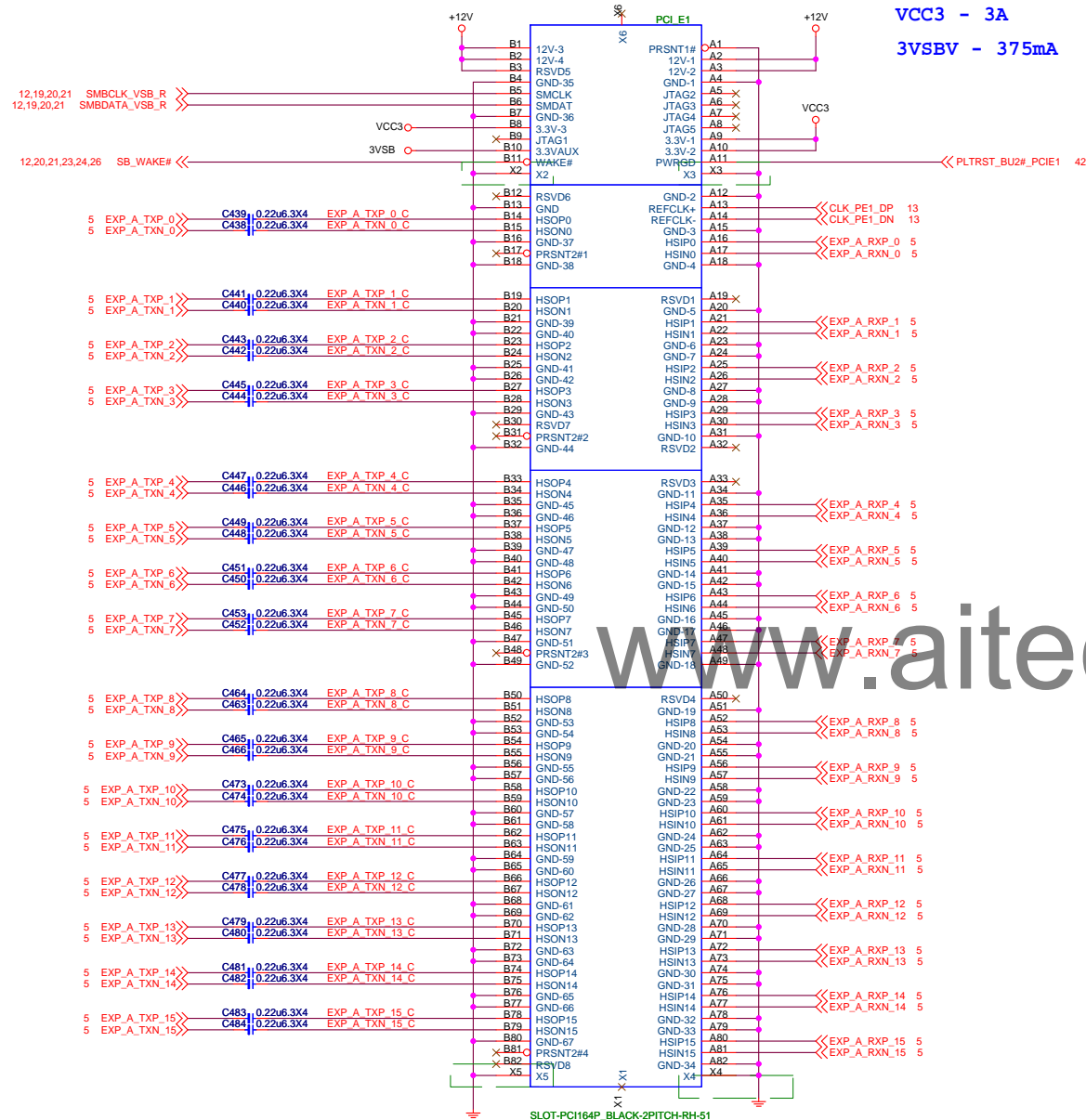
12V - 5.5A
VCC3 - 3A
3VSBV - 375mA

SMBUS ESD

SMBCLK_VSB_R R435 4.7K0402 3VSB
SMBDATA_VSB_R R436 4.7K0402 3VSB

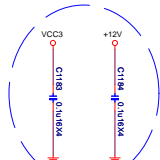
**By Placement**

Main:D0G-05A0529-A68
AVL:D0G-45B0510-114

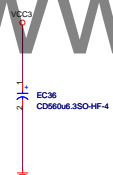
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PCI_Express X4 Slot



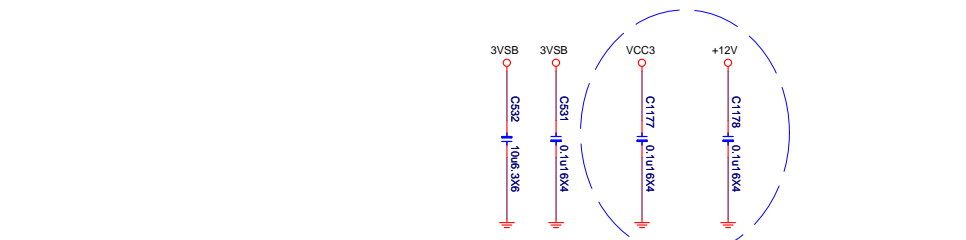
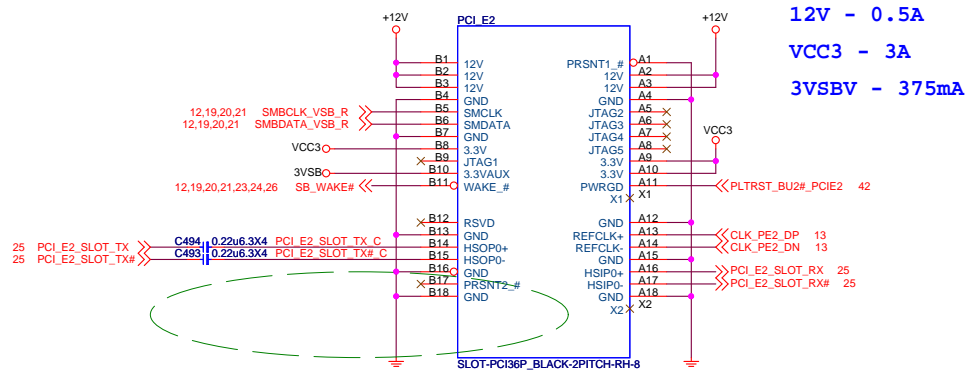
PCI_Express X4 Slot



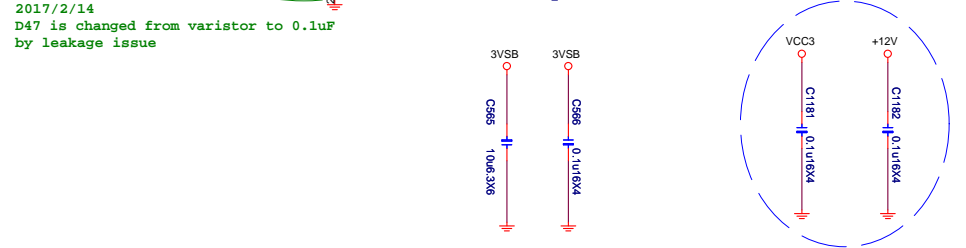
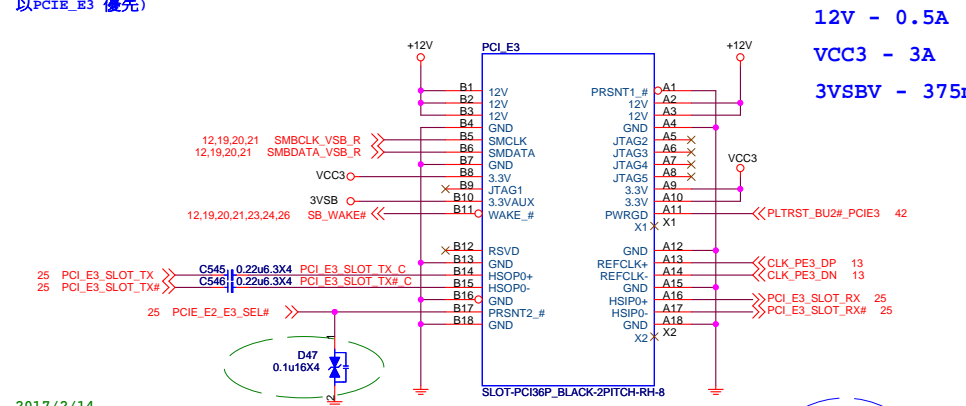
A circuit diagram showing a 12V DC voltage source connected in series with a diode. The diode is labeled EC35 CD270u16SO-HF-11. The circuit is drawn with red lines on a white background.



N11-0360211-F02/N11-0360381-L06 (與PCIE_E2 & PCIE_E3互切, PCIE_E2 & PCIE_E3同時有PCIE device 以PCIE_E3 優先)

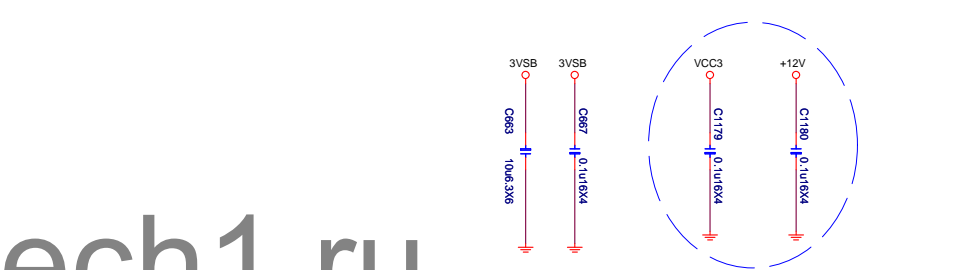
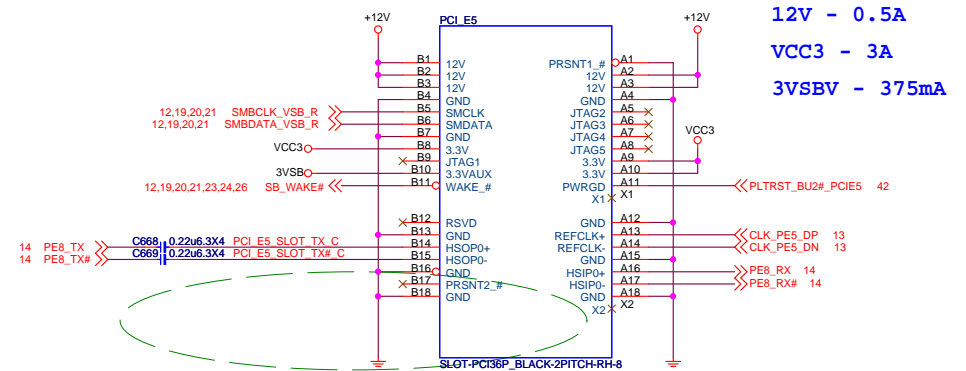


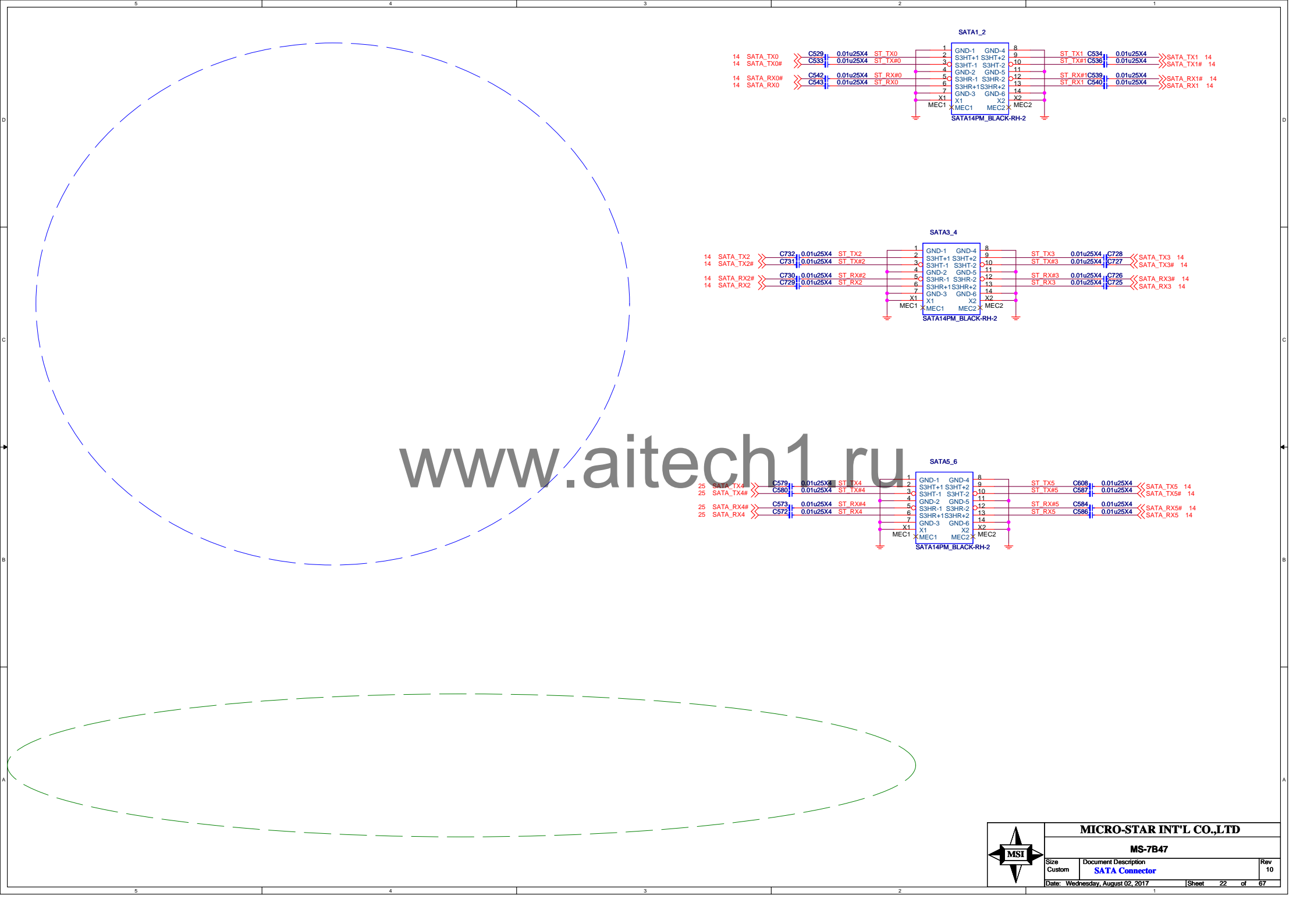
N11-0360211-F02/N11-0360381-L06 (與PCIE_E2 & PCIE_E3互切, PCIE_E2 & PCIE_E3同時有PCIE device 以PCIE_E3 優先)



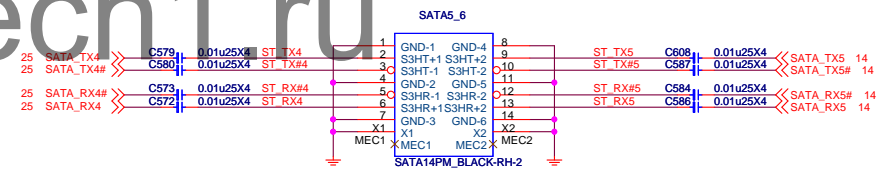
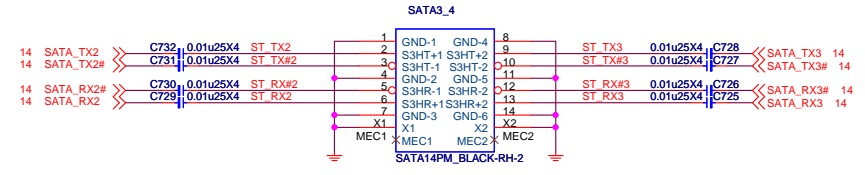
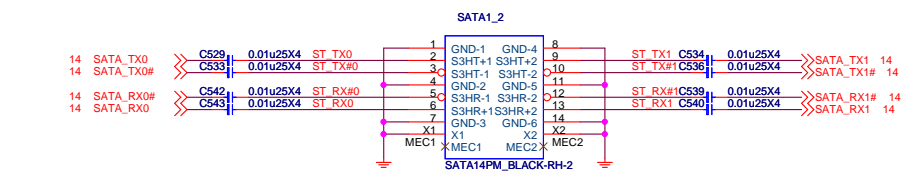
2017/2/14
D47 is changed from varistor to 0.1uF
by leakage issue

(PCIE_E5 獨立使用PE8_TX/RX)

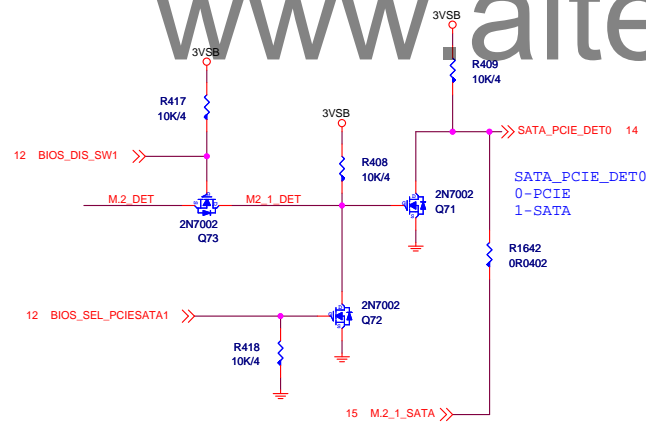
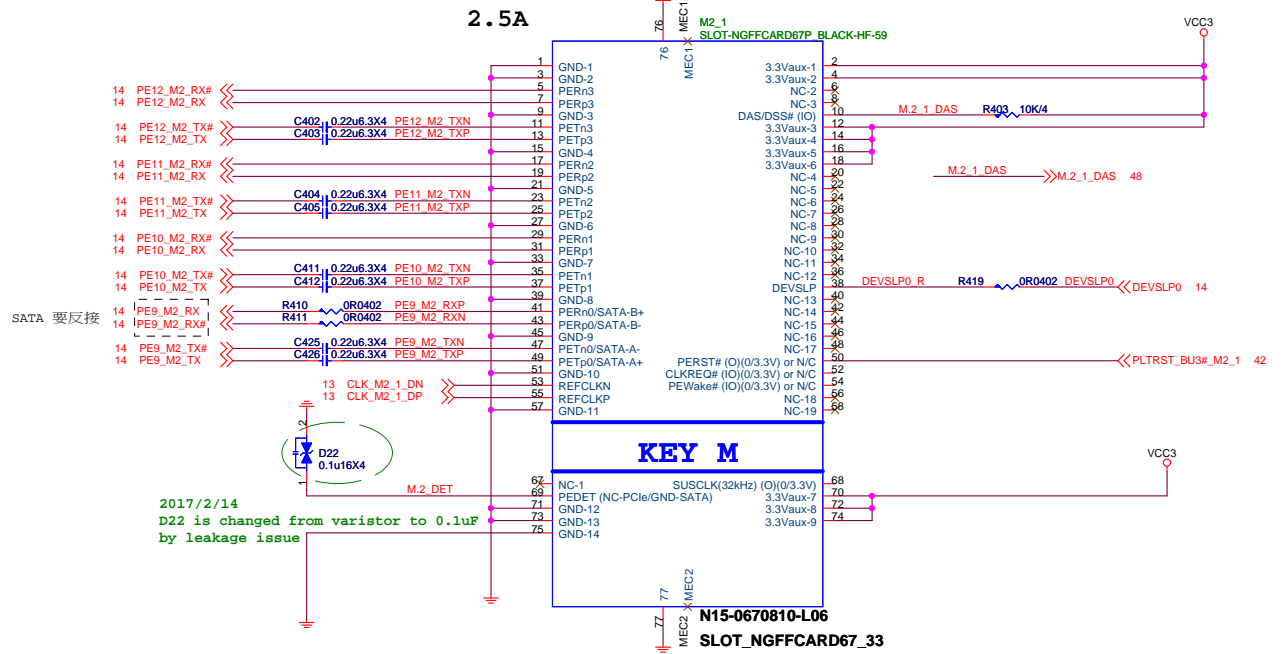




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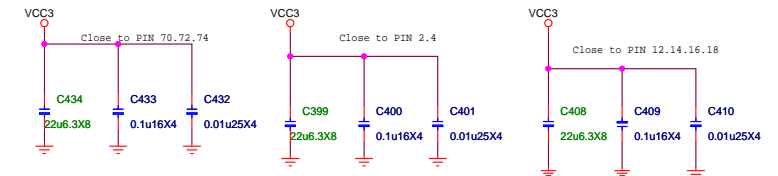
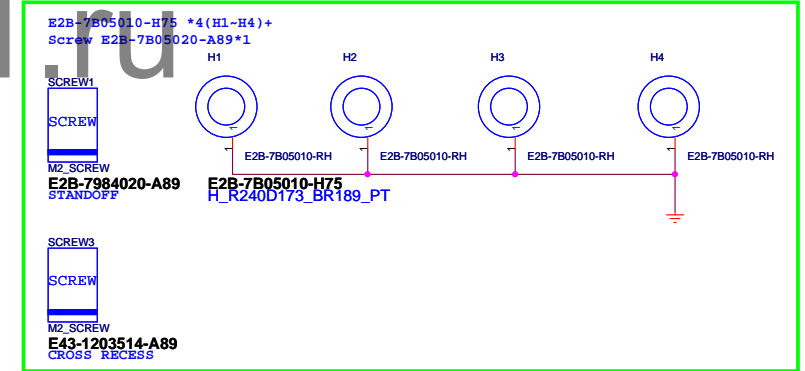
MICRO-STAR INT'L CO.,LTD			
MS-7B47			
Size	Document Description		Rev
Custom	SATA Connector		10
Date: Wednesday, August 02, 2017		Sheet	22 of 67

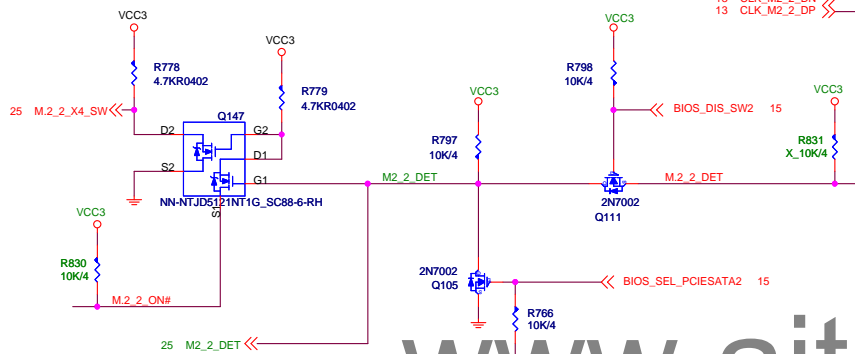
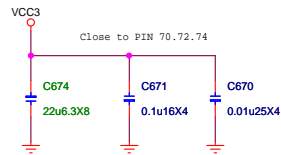
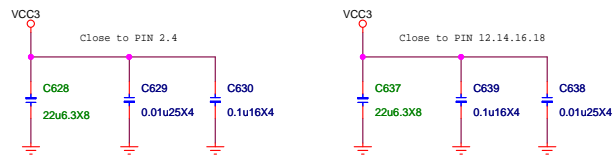


BIOS_MODE

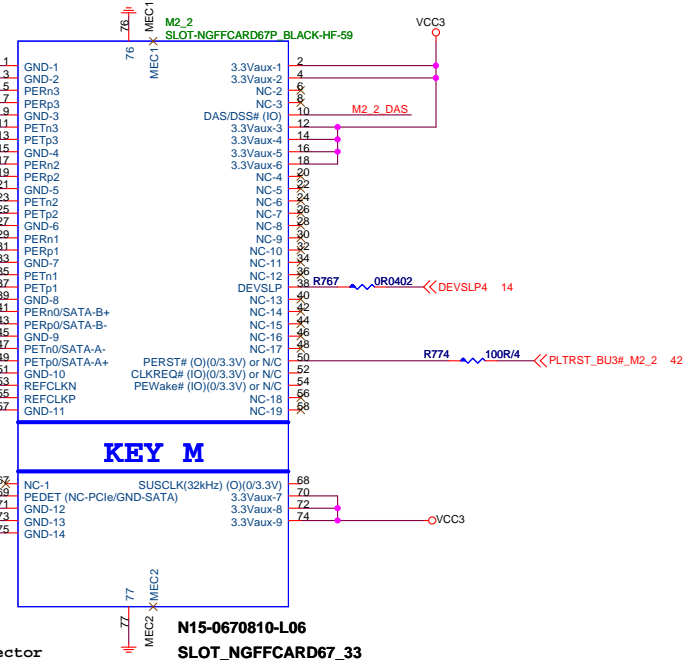
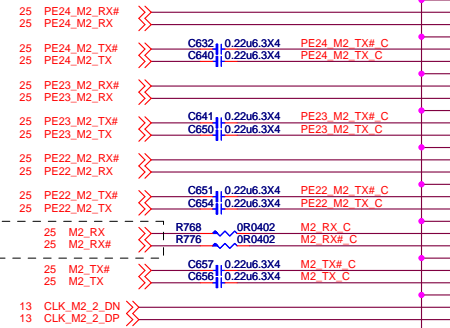
BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

2017/6/22 modification





SATA 要反接



KEY M

N15-0670810-L06
SLOT_NGFFCARD67_33

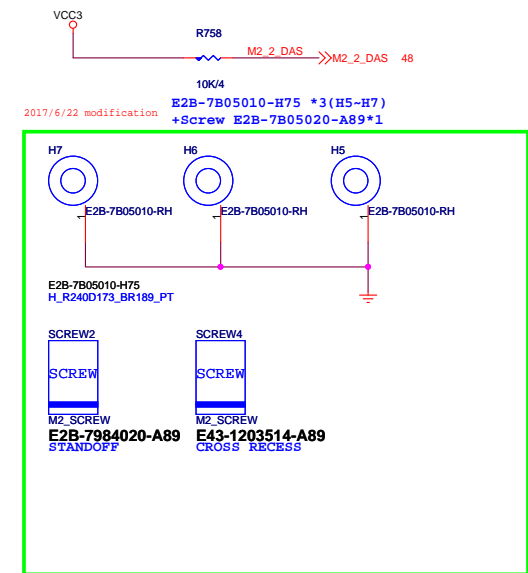
D30,D31 Close to M2 connector
2017/2/14
D30, D31 are changed from varistor to 0.1uF
by leakage issue

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Pin	BIOS_SEL_PCIESATA2	BIOS_DIS_SW2	M.2_2_DET	M.2_2_ON#	M.2_2_DET	M.2_2_SATA	M.2_2_X4_SW	M.2_2_PCIE	M.2_2_Status	SATA port5	PCIe x 4
GPIO	GPP_G5	GPP_G7	X	X	X	GPP_A20	X	GPP_A19	X	X	X
X	0	1	H	L	H	1	H	1	M.2 PCIe type	Active	Inactive
X	0	1	L	L	L	0	L	0	M.2 SATA type	Inactive	Active
X	0	1	H	H	H	1	L	0	X	Active	Active
Pin	BIOS_SEL_PCIESATA1	BIOS_DIS_SW1	M.2_DET	X	M.2_1_DET	M.2_1_SATA	X	X	M.2_1_Status	SATA port1	X
GPIO	GPP_H13	GPP_H15	X	X	X	GPP_A18	X	X	X	X	X
X	0	1	H	X	L	0	X	X	M.2 PCIe type	Active	X
X	0	1	L	X	H	1	X	X	M.2 SATA type	Inactive	X
X	0	1	H	X	L	0	X	X	X	Active	X

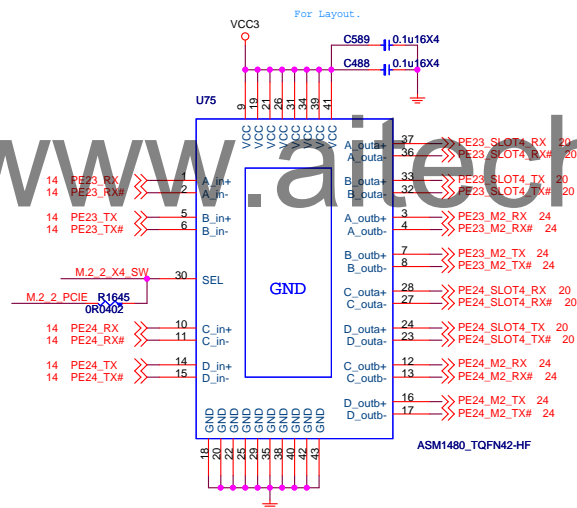
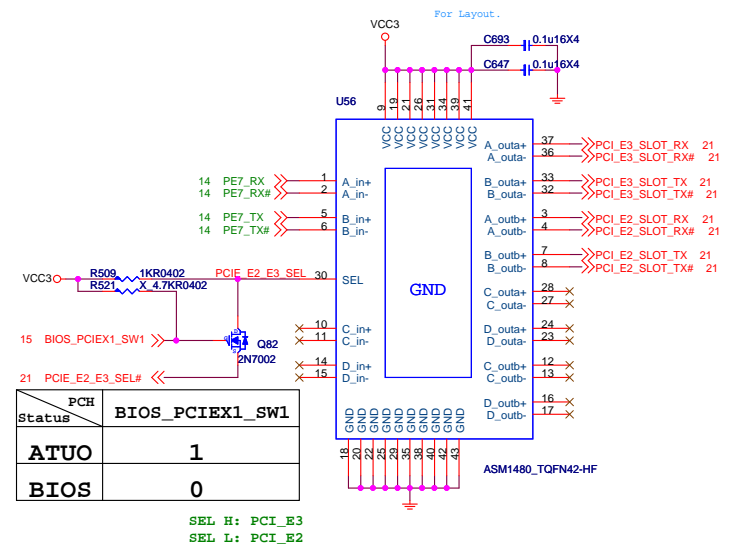
SATA_PCIE_DET4
0-PCIE
1-SATA

PCH side
0:PCIE
1:SATA
M.2 side
0:SATA
NC:PCIE



BIOS_MODE

BIOS_DIS_SW2	BIOS_SEL_PCIESATA2	Mode
1	0	M2-PCIE
0	1	X4 SLOL-PCIE
GPI	GPI	GPI



M.2_2 SATA

M2_2_ON	M.2_2_X4_SW	M.2 SATA	M.2 PCIE	X4 SLOT	SATA5
V	V	X	X	V	V
X	X	X	V	X	V
X	V	V	X	V	X



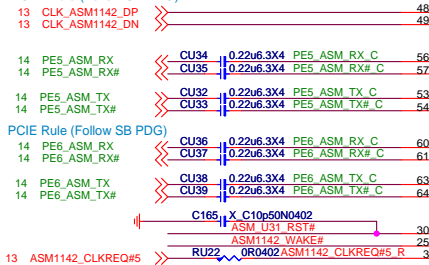
MICRO-STAR INT'L CO.,LTD			
MS-7B47			
Size Custom	Document Description M.2/SATA/PCIE SW		Rev 10
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Minimum gap should be greater of
>15mil with other signal.

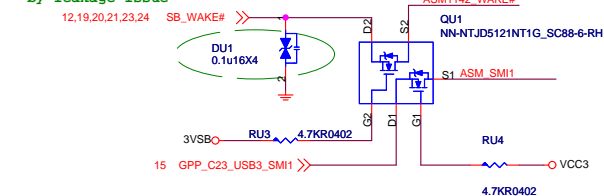
USB HS (90Ohm-Diff) Chip to Connector 1.5 inch.

CLK Rule (Follow SB PDG)



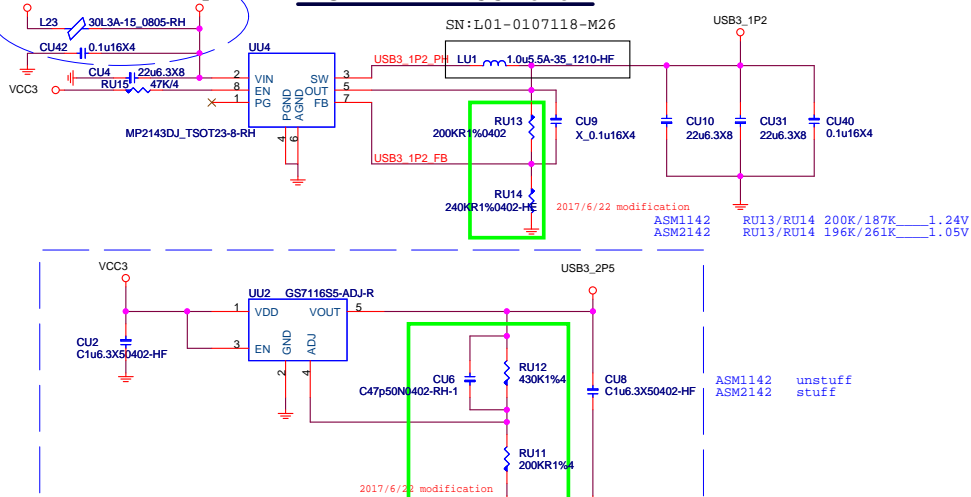
SMI connect to GPI which support smi function. SB side pull high 10K ohm to 3VSB. (Intel 8X & 9X series use GPIO10) (Intel SKL use GPP_C23)

2017/2/14
DU1 is changed from varistor to 0.1uF by leakage issue

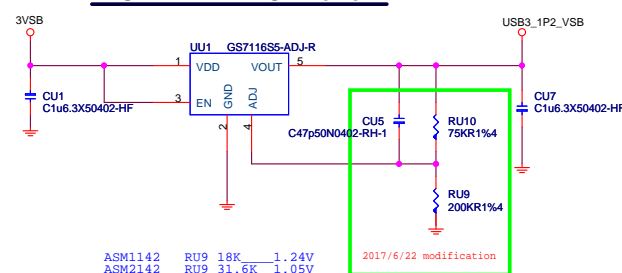


atx5vab change to vcc5
ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

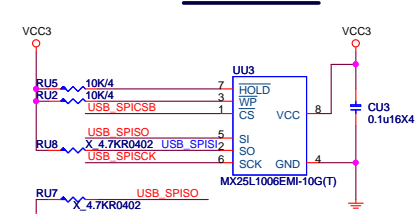
ASM1142 1.2 VCC Power



ASM1142 1.2 VSB Power



EEPROM



2016 . 7 . 20

ASM1142 U03 M31-2551222-M24(512K bit)
ASM2142 U03 M31-2551022-M24(1M bit)

MICRO-STAR INT'L CO.,LTD

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Custom	ASM 1142	10
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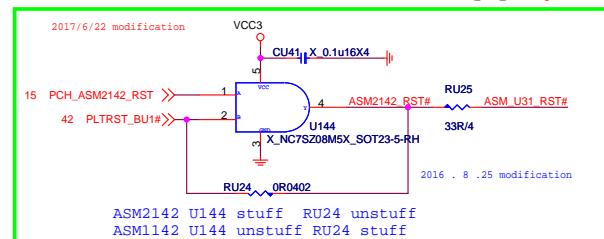
Power Consumption

	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	250mA	650mA	56mA	15mA	NA	1573.8(mW)
ASM2142	4mA	470mA	9mA	10mA	220mA	TDP

3142

Layout Guide:

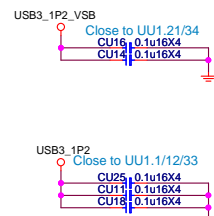
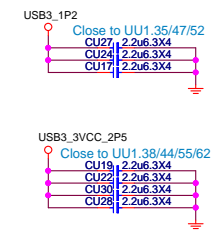
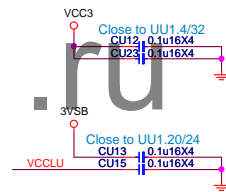
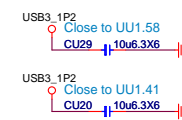
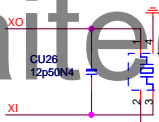
- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2



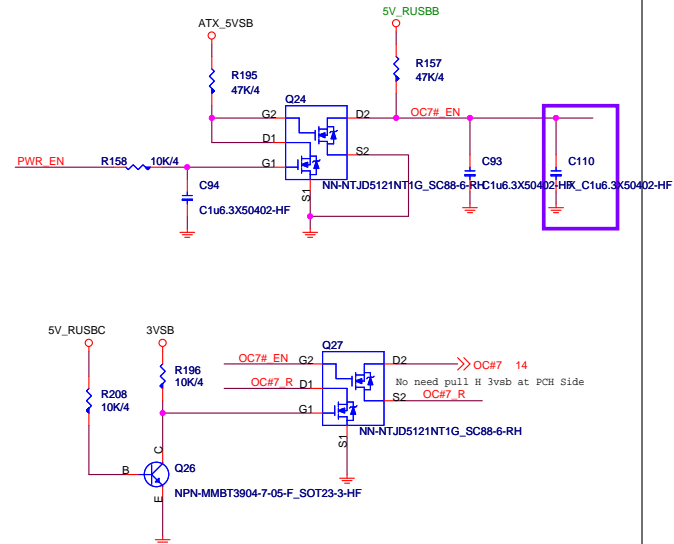
X0/X1 (95hm-Diff, Spacing 30mil)

UREXT, PEUREXT(W/S) : 10/7

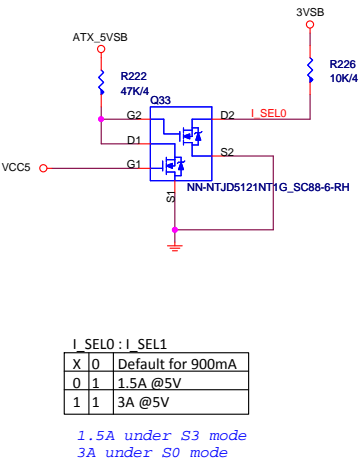
OCIA, OCIB, PPOA, PPOB(W/S) : 5/8



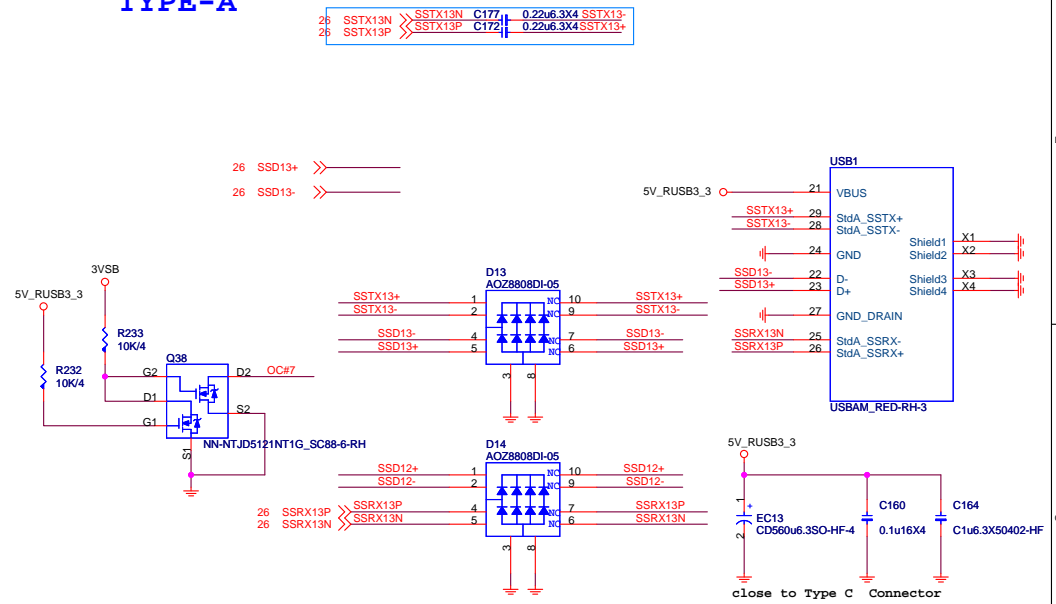
VBUS OC#



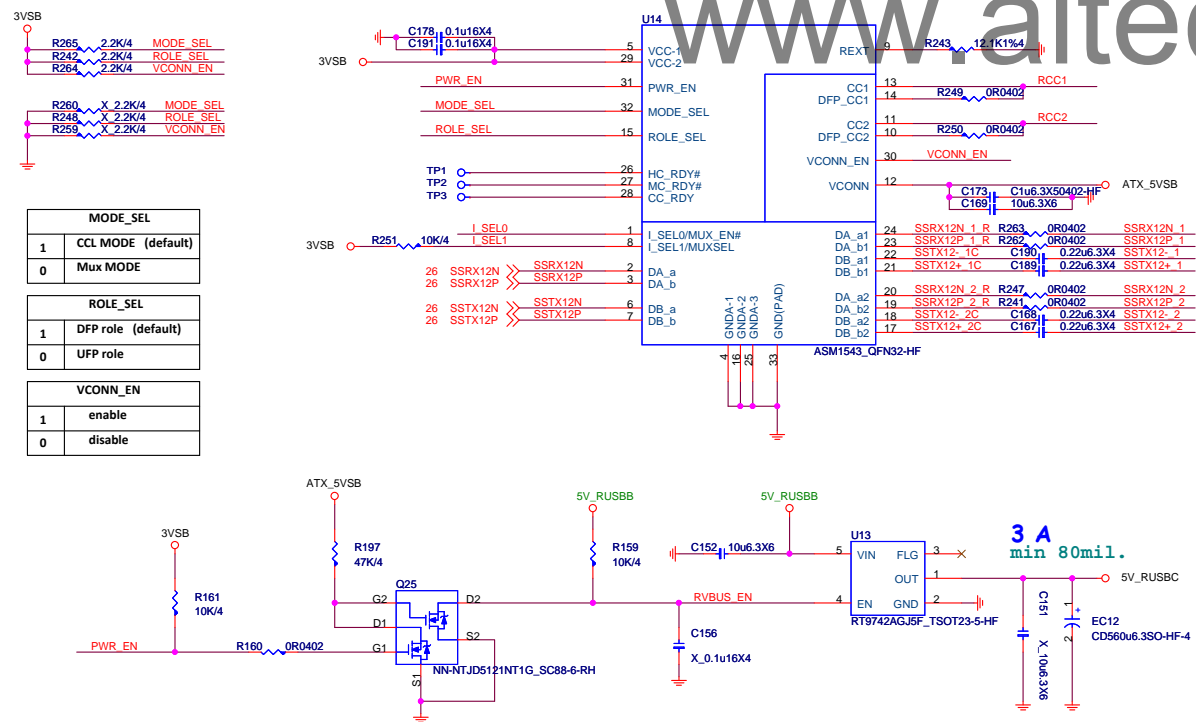
Current Mode



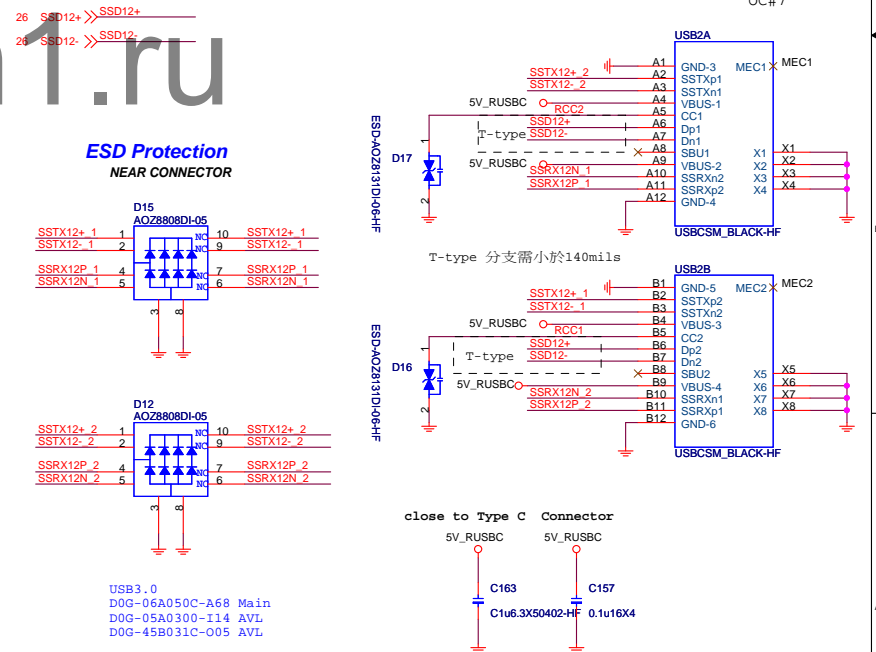
TYPE-A



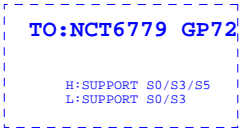
USB Type-C MUX with Configuration Channel (CC)



TYPE-C



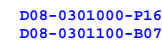
USB PORT POWER



REAR USB PORT POWER

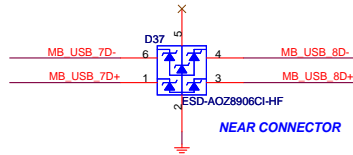
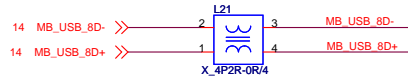
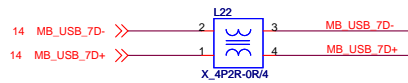


FRONT USB PORT POWER

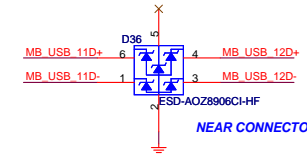
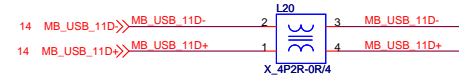
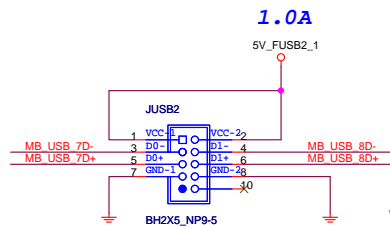


N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

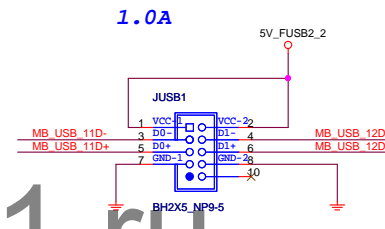
VR 1.5A*2



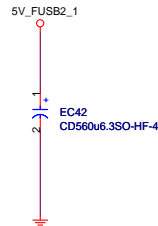
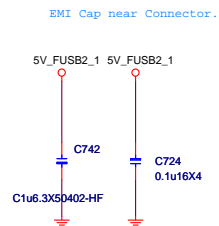
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14



Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

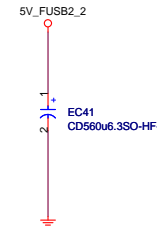


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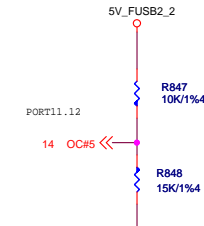
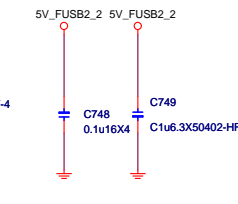


PORT7.8

14 OC#3



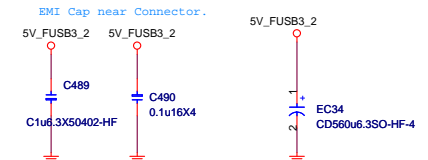
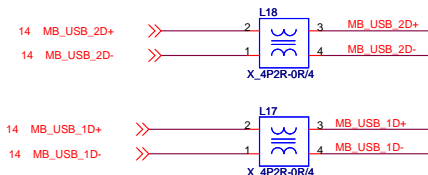
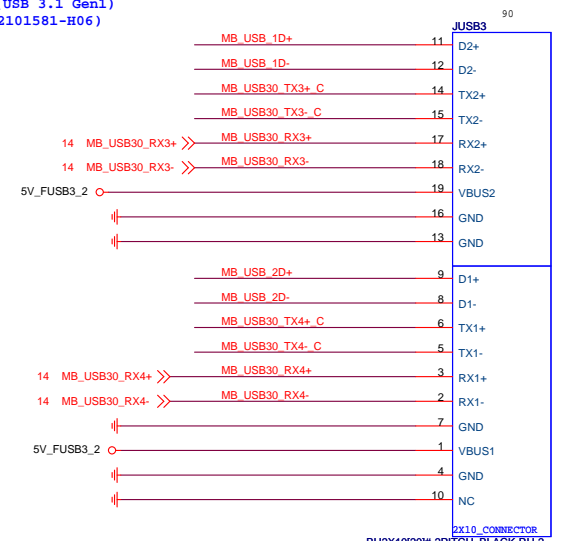
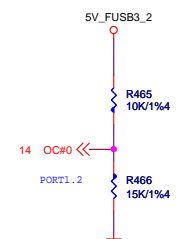
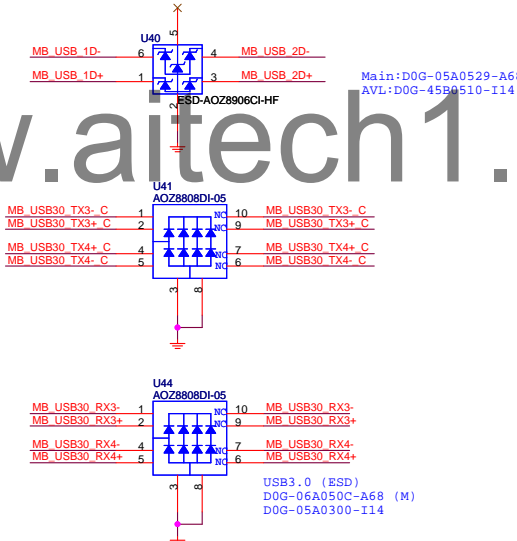
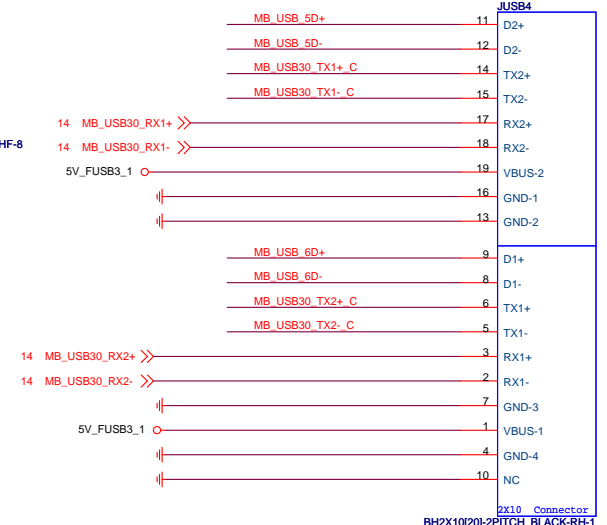
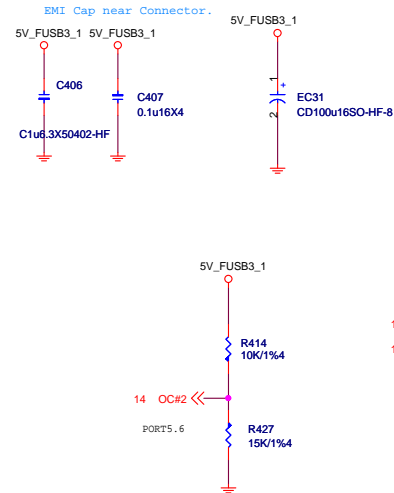
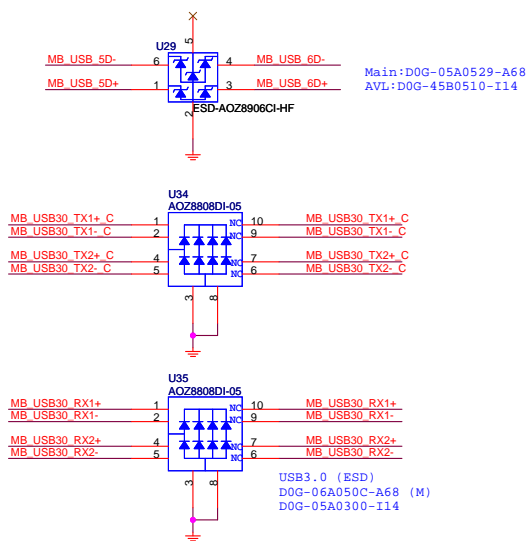
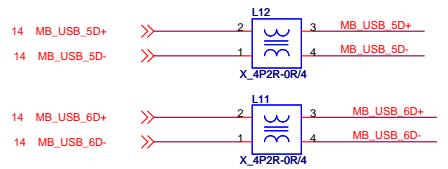
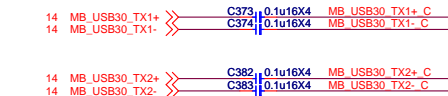
EMI Cap near Connector.



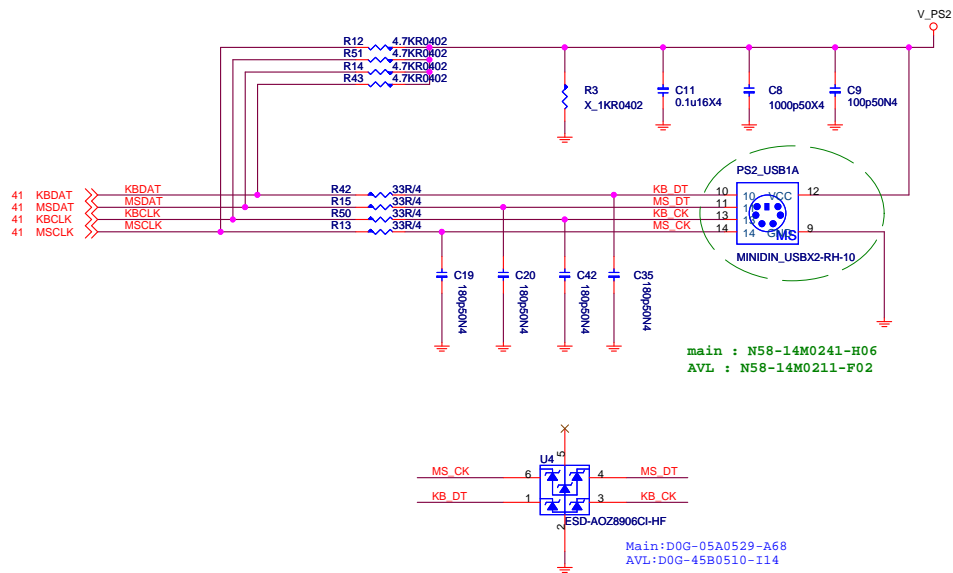
MICRO-STAR INT'L CO.,LTD

MS-7B47

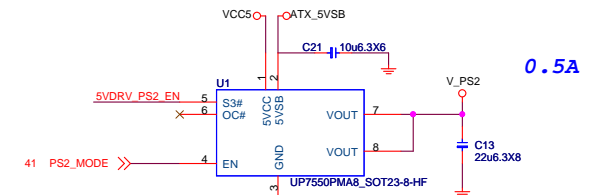
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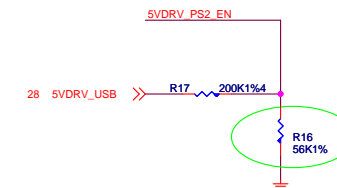
PS2 Connector



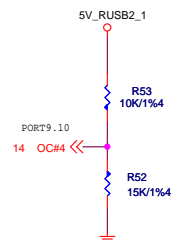
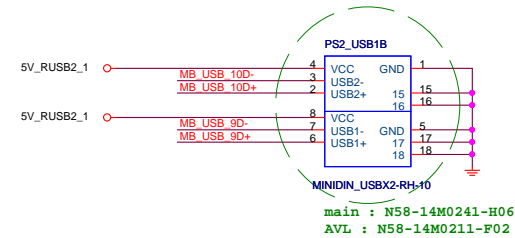
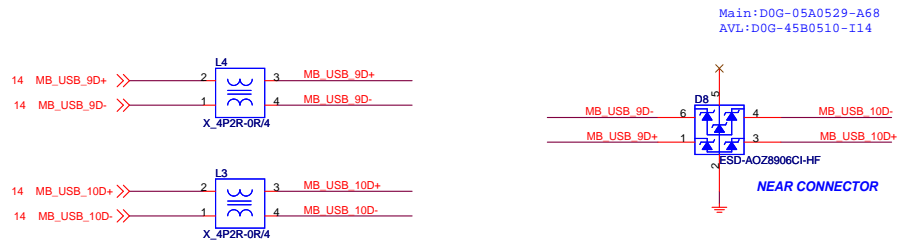
PS2 Power



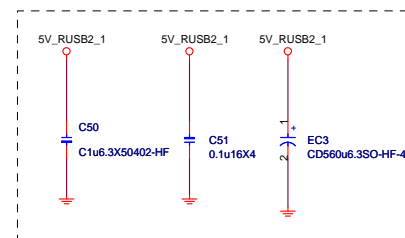
USB MODE



PS2 _USB



Close to Connector



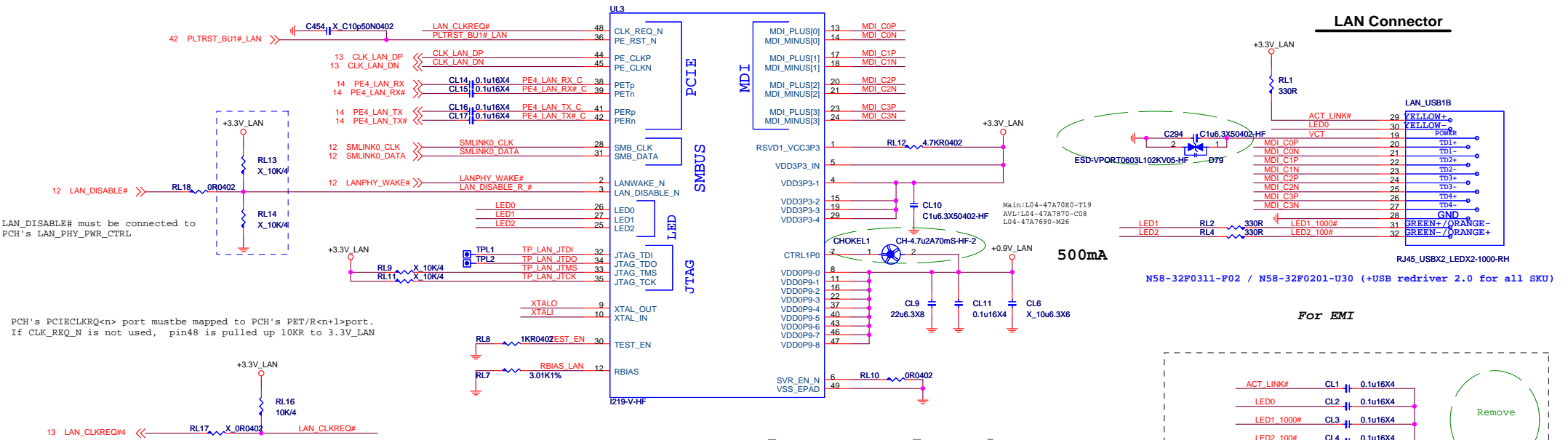
MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	Real USB2&PS2 CONNECTOR	10
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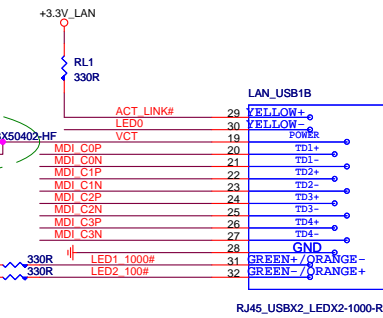
Intel Lan- i219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09



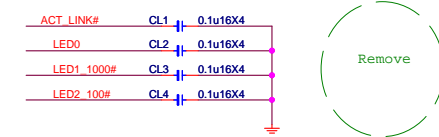
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LAN Connector

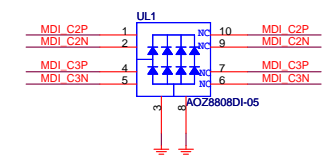
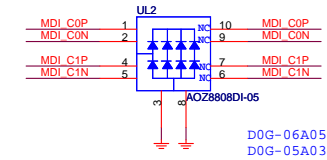


N58-32F0311-F02 / N58-32F0201-U30 (+USB redriver 2.0 for all SKU)

For EMI

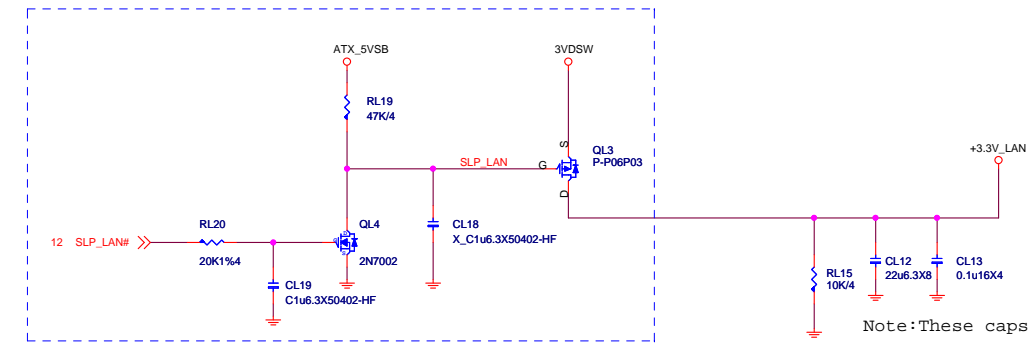


UL2&UL3 close to connector



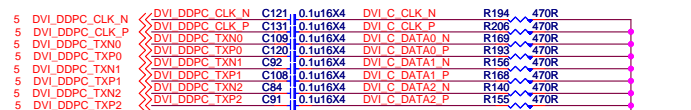
+3.3V LAN

I218:132mA
I219:542mW

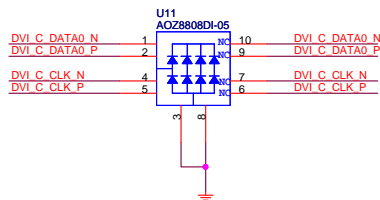


MICRO-STAR INT'L CO.,LTD			
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Custom	Intel Lan- i219	10	
Date: Wednesday, August 02, 2017	Sheet	33	of 67

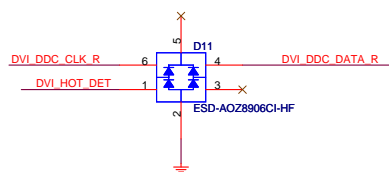
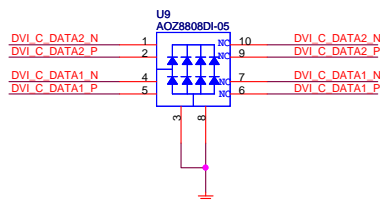
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



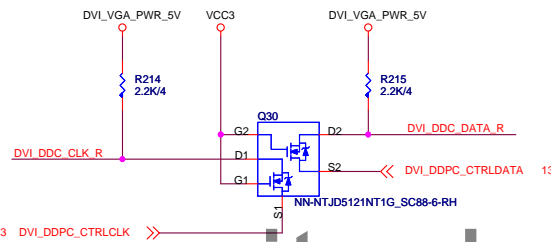
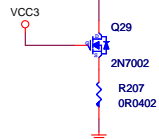
U26 AVL:D0G-05A050C-005
D0G-06A050C-A68



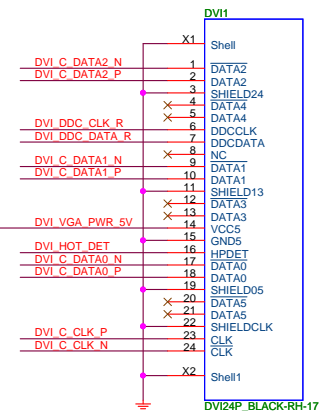
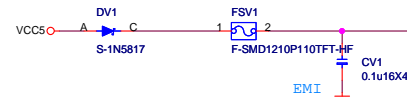
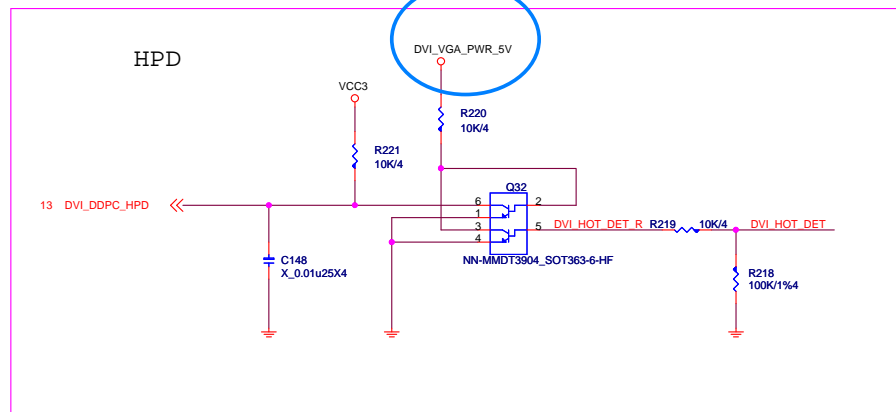
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D0G-06A050C-A68



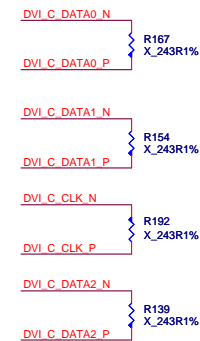
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14



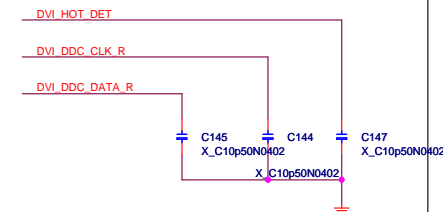
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For EMI



EMI

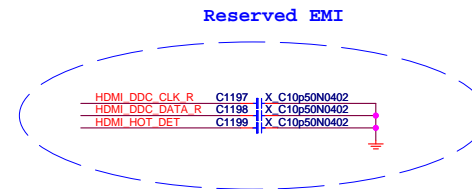
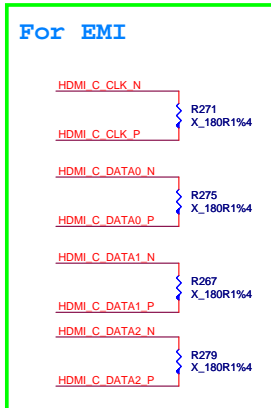
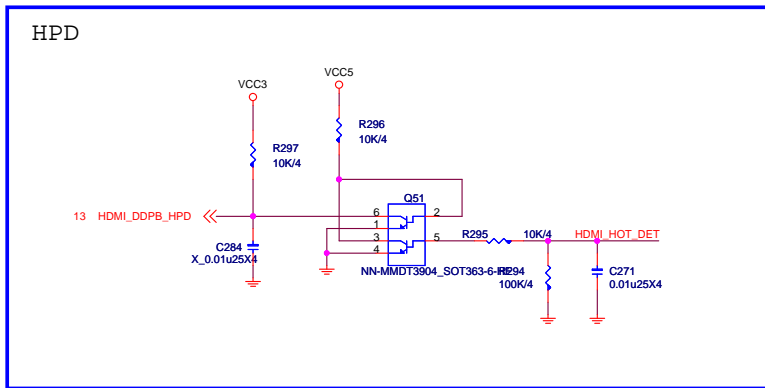
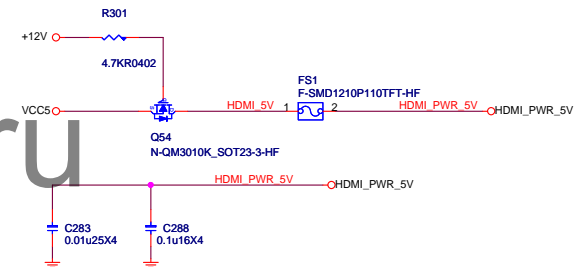
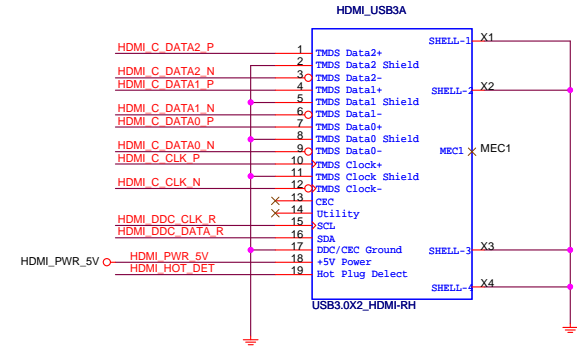
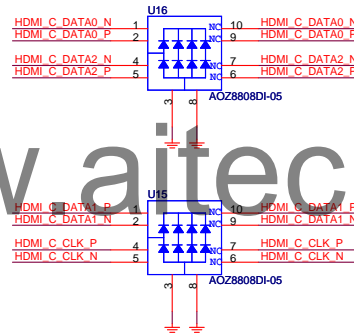
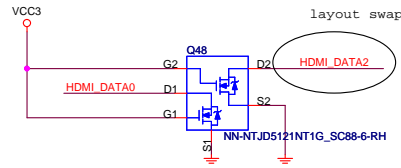
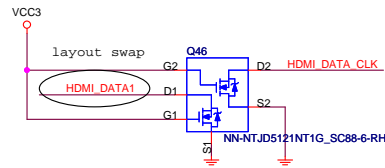
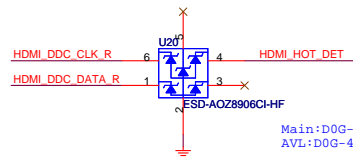
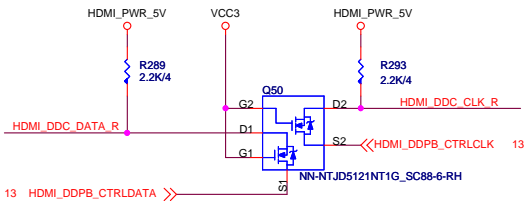
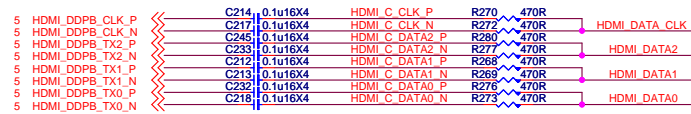


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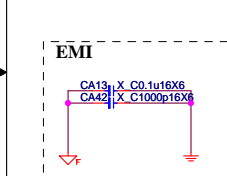
Size	Document Description	Rev
Custom	DVI Connector	10
Date: Wednesday, August 02, 2017	Sheet 34 of 67	

HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

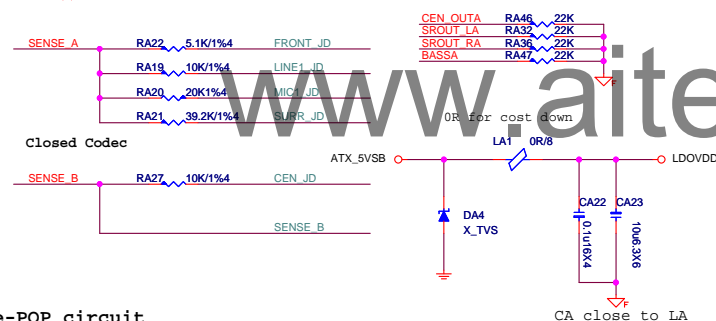


2015.04.24 Modify from
ALC1150 to ALC892

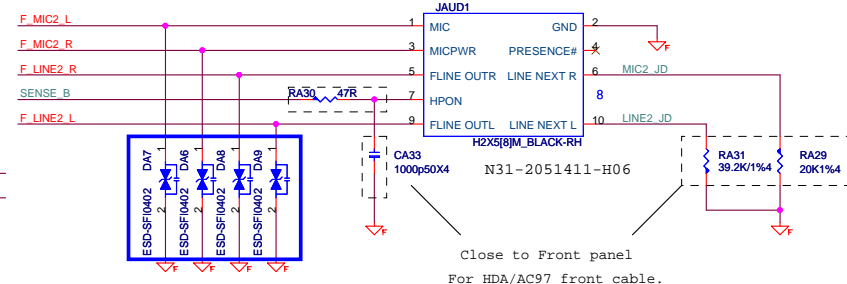
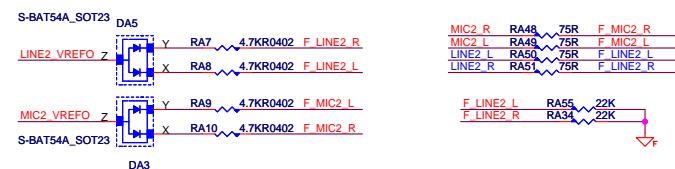
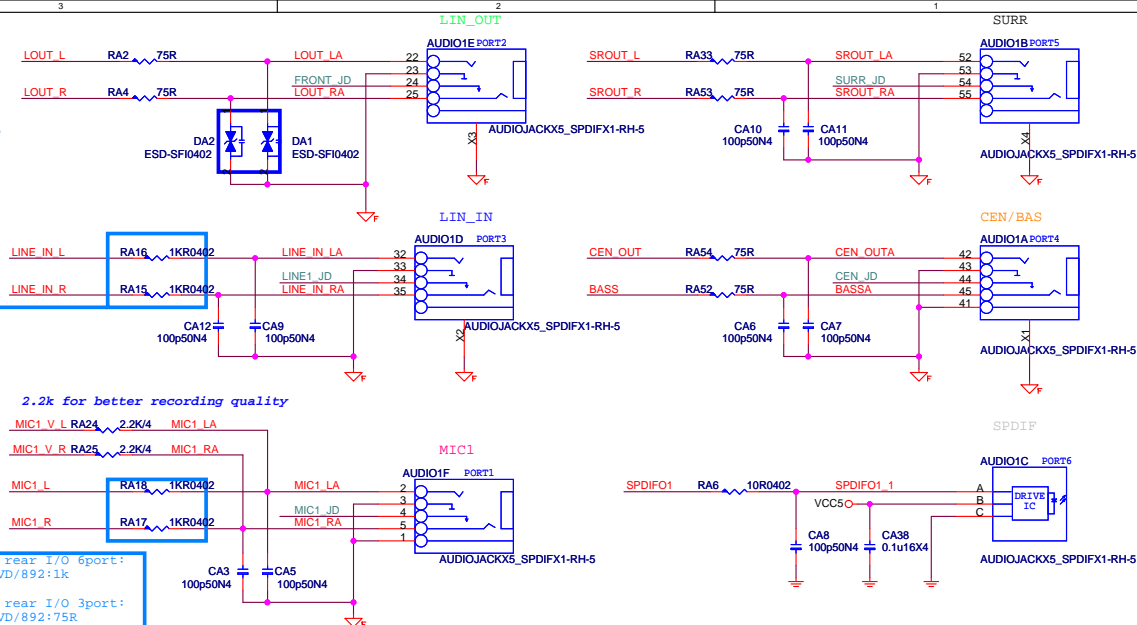
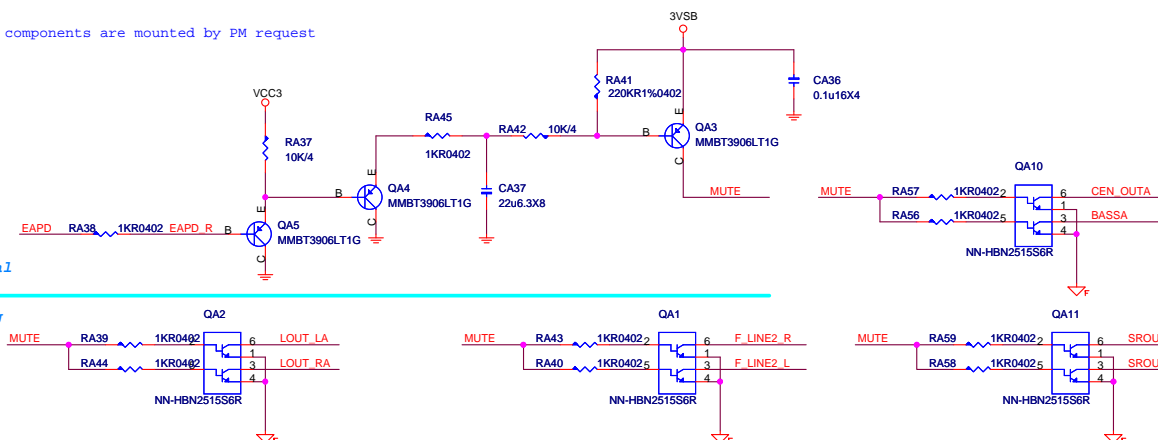
13 AZ_SDOUT
13 AZ_SDINO
13 AZ_SYNC
13 AZ_RST#



All components are mounted by PM request



Analog



Varister --> cap for cost down

D0G-2950500-SI0
D0G-3010510-I05
Close to Jack



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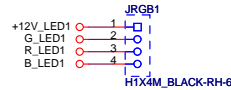
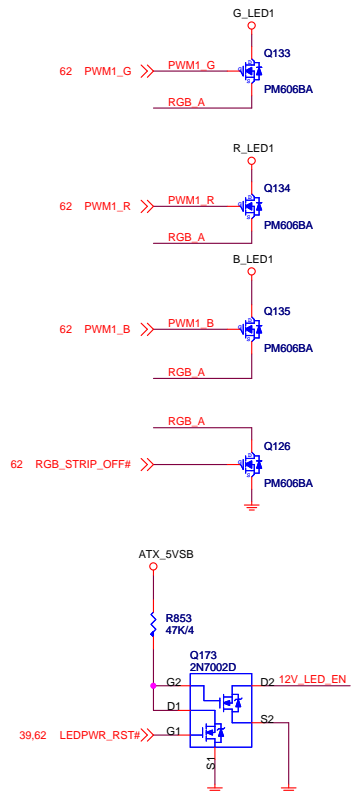
MS-7B47

Size	Document Description
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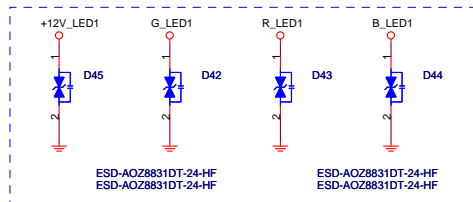
Custom	AUDIO ALC892
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	Rev 10
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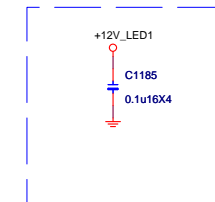
LED STRIPLINE(LEFT)



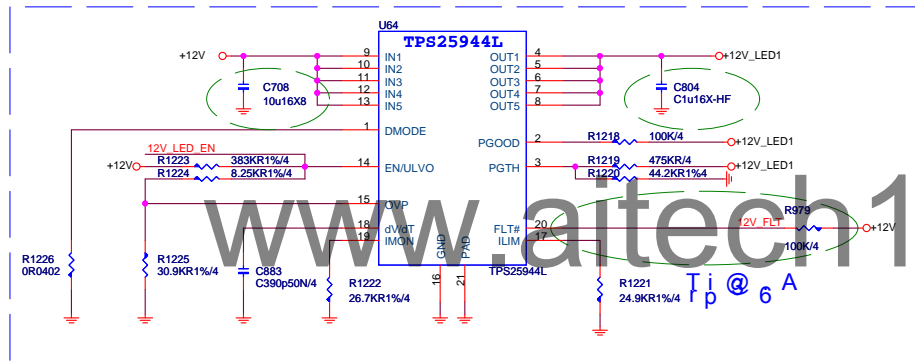
2016.08.02 stuff ESD
2016.07.06 only reserve now
2017.03.06 ESD change to used D0G-35B240C-A68



2016.08.02 Add +12V_LED 0.1uF

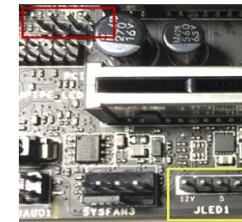


2016.07.06 Use TPS25944L



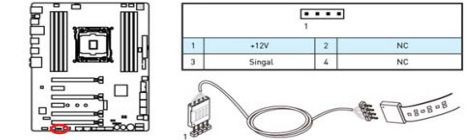
位置統一於下板邊

RGB : (參考7A20) , 單色 : (參考7A45) 方便USER 操作 *若走線遇到困難時 , 再另外提出討論*
使用MCU就必須搭配 J11 燒錄FW的Connect (如紅框)
PCB 文字面 & 手冊說明如下:



JLED1: LED connector

This connector allows you to connect the single color LED strip.



Important

- This connector supports 5050 single-color LED strips with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.
- Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.
- Please use the **LED Effect** of GAMING APP to control the LED light, refer to the Software section for details.

外接LED 燈條 (RGB)

---- PCB 文字面 (JLED1)

---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺 (待7A20驗證)

DIMM_SLOT

TOMAHAWK (Z270) / CAMO SQUAD(Z270)
紅 : X (1.0) / X (4.0)
KRAIT GAMING (B250)
白 : M:D0C-040T200-H91 / S:D0C-040S200-E07*4
TOMAHAWK ARCTIC(H270)
X (1.0)

需做紅白LED colay 線路 . 因VF值不一樣 , 供電的電壓要特別注意

LED 命名請以DIMM_LEDn n為數字

HW Detect+SIO 說明
HW Detect
DIMM1/2/3/4
-->DIMM PIN2 control
SIO 呼吸
-->SIO PIN98(MLED/GP27)
ALL LED ON/OFF
-->SIO PIN98(MLED/GP27)

PCI_SLOT_LED

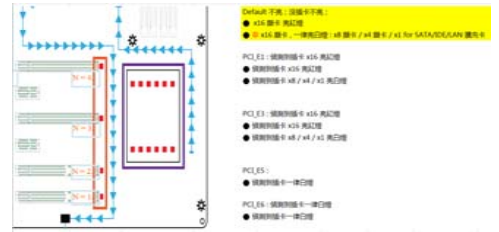
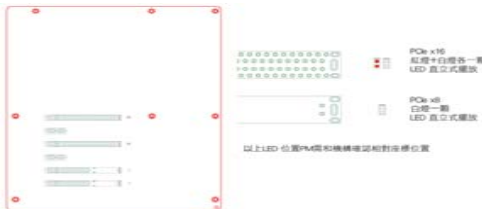
TOMAHAWK (Z270) / TOMAHAWK ARCTIC(H270) / CAMO SQUAD (Z270)
PCIE x16 : X(1.0) / X(2.0) / X(4.0)
KRAIT GAMING (B250)
PCIE x16 紅 : M:D0C-040P100-H91 / S:D0C-040S500-E07*1
白 : M:D0C-040T200-H91 / S:D0C-040S200-E07*1


TOMAHAWK (Z270) / TOMAHAWK ARCTIC(H270) / CAMO SQUAD (Z270)
PCIE x4 : X(1.0) / X(2.0) / X(4.0)
KRAIT GAMING (B250)
PCIE x4 白 : M:D0C-040T200-H91 / S:D0C-040S200-E07*1

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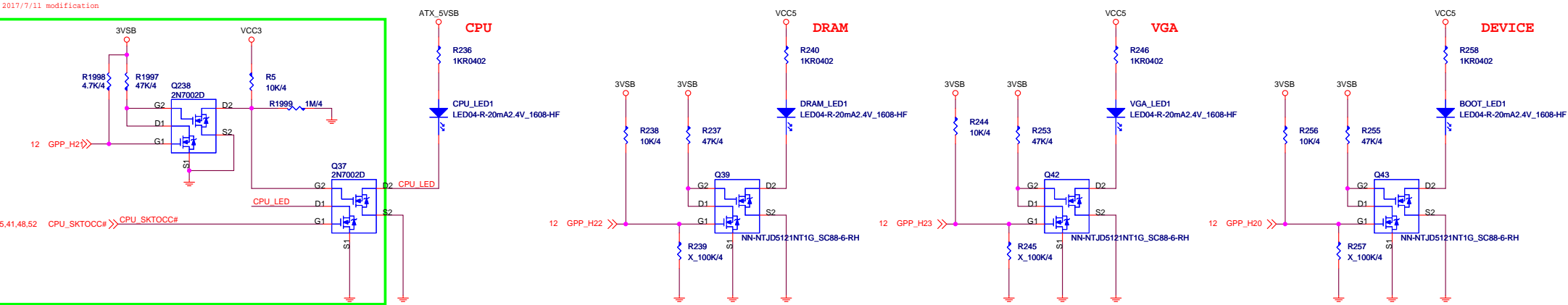
PCIE SLOT4

PCIEx16 & x8(可切X16/X8的X16 SLOT) : GPIO X2/呼吸控制
高階(M5/M7/M9/XPOWER)有加GPIO CONTROL IC(5605)在確認
其他切換的GPIO
-->紅/PCH GPP_C8
-->白/PCH GPP_C9
-->呼吸控制-->SIO PIN98(MLED/GP27)
-->ALL LED ON/OFF-->SIO PIN98(MLED/GP27)
其他X16 SLOT : HW Detect/呼吸控制
HW DETECT
-->PCIE PRSENT控制
呼吸控制
-->SIO PIN98(MLED/GP27)
ALL LED ON/OFF
-->SIO PIN98(MLED/GP27)



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	Size Custom	Document Description LED DIMM/PCIE	Rev 10
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EZ DEBUG LED



開機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. 因此最後正常順利開機後，三個LED燈都是減掉的。

(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

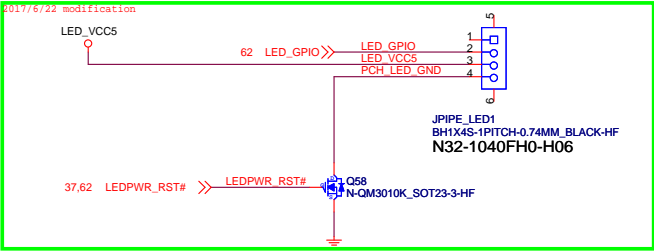
位置統一於右側JFWR1上方區塊 (參考 7A20) *若走線遇到困難時，再另外提出討論*
需做紅白LED colay 線路。因VF值不一樣，供電的電壓要特別注意

LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

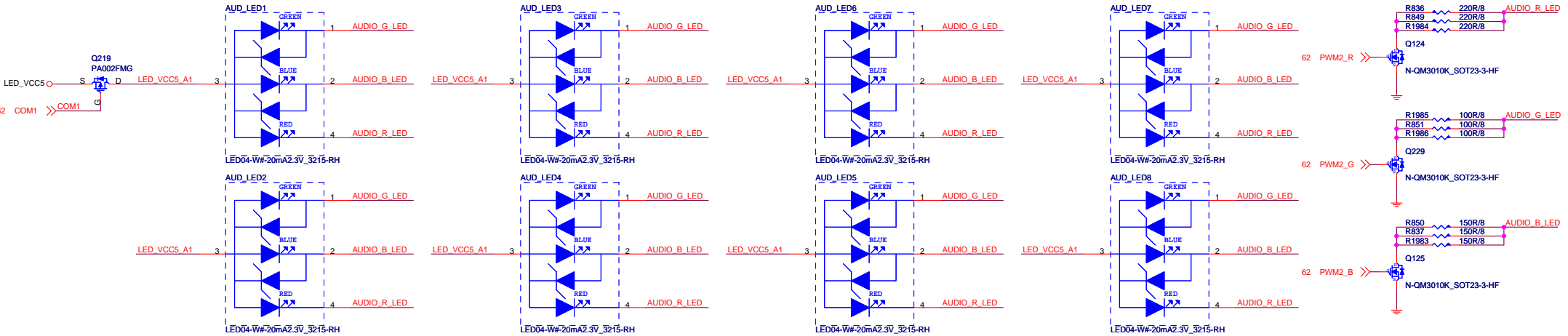


PCH Heatsink color LED

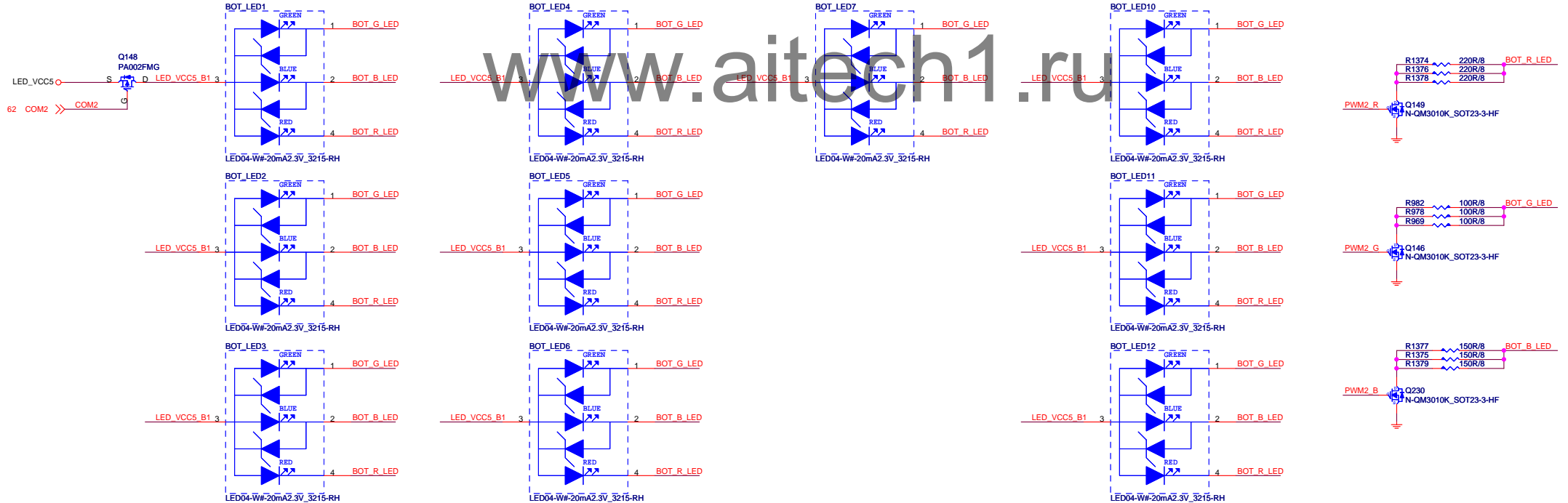
PIPE_VCC5 > 20mil
PIPE_VCC5 please check your Heatsink LED USE
單色：電流0.02 A x 總燈數

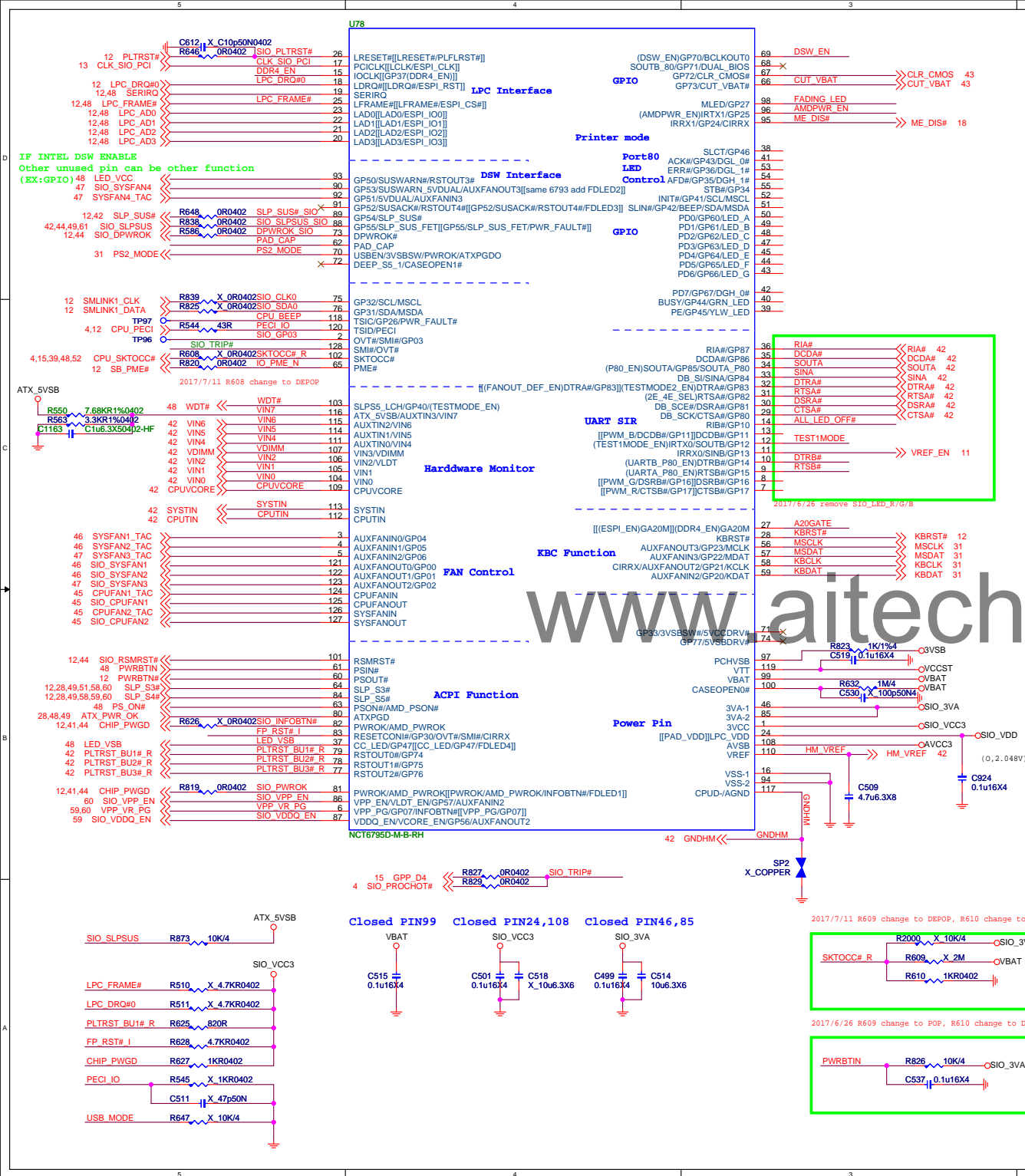


AUDIO RGB LED Audio moat is transparent and width 40mil



BOTTOM LED





DSW_EN R687 X 0R0402

AMDPWR_EN R630 X 0R0402

SLP_SUS# SIO R942 X 10K/4

R654 X 100K/4

USB_MODE 28

CUT_VBAT

CUT_VBAT 43

FADING_LED

ALL_LED_OFF# R761 47K/4

SIO_VPP_EN R588 4.7K/0402

SIO_VDDQ_EN R585 4.7K/0402

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO

3V Analog Power

Intel 6793 pull down 6795 pull down

6793 DDR4_EN strapping 6795 ESPI_EN strapping

Intel 6793 pull high 6795 LPC pull down/ESPI pull high

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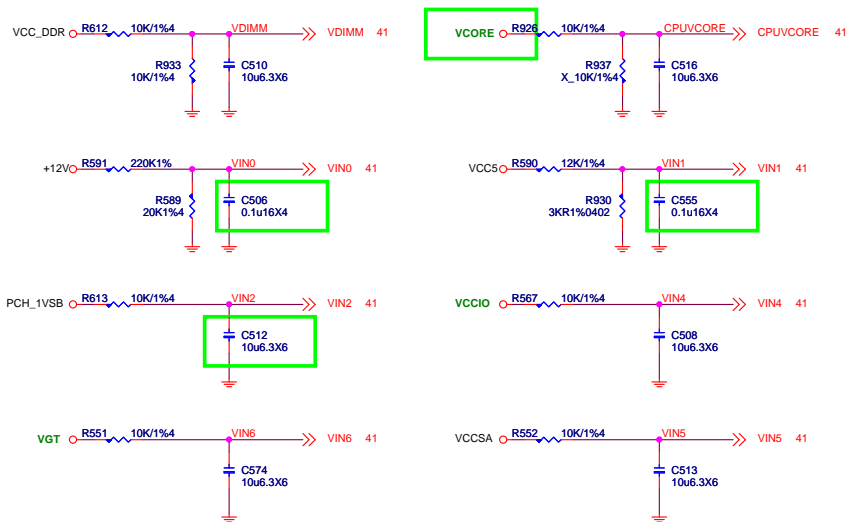
MS-7B47

Size	Document Description	Rev
Custom	SIO-NTC6795D-1	10

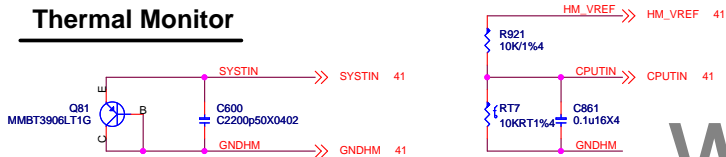
Date: Wednesday, August 02, 2017 Sheet 41 of 67

HW Monitor - Voltage

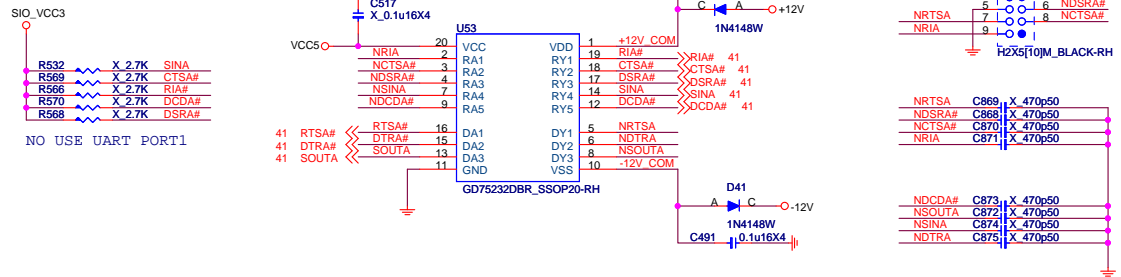
SIO HM Voltage voer 2V will not detect



Thermal Monitor



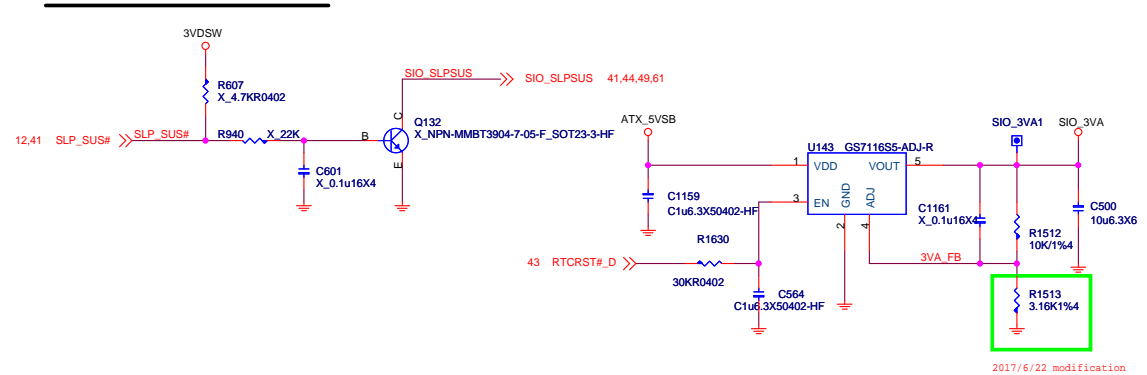
SERIAL PORT 1



PARALLAL PORT

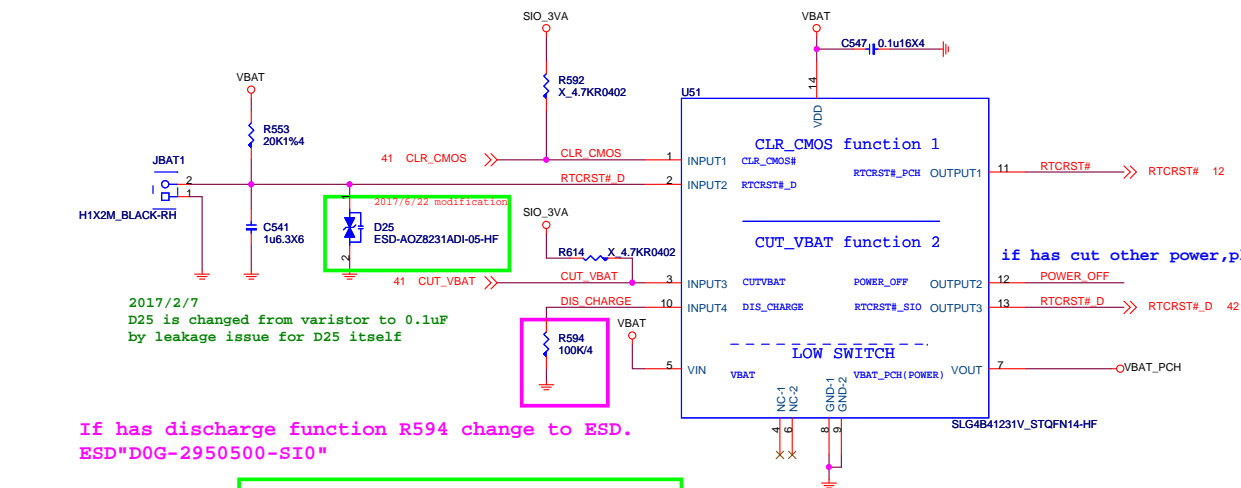
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SLP_SUS Co-lay circuit

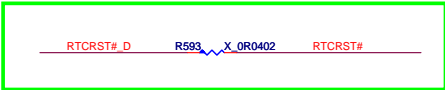
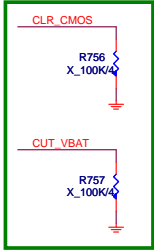


CLR_CMOS

VBAT



20160629



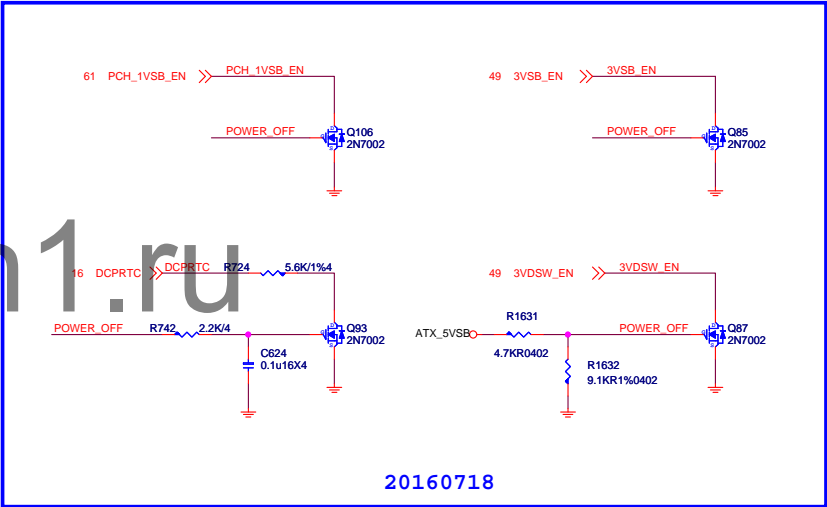
Co-Lay NOT USE U12 , R139 STUFF
If STUFF R139 Please Check RTCRST# Double Pull High

Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

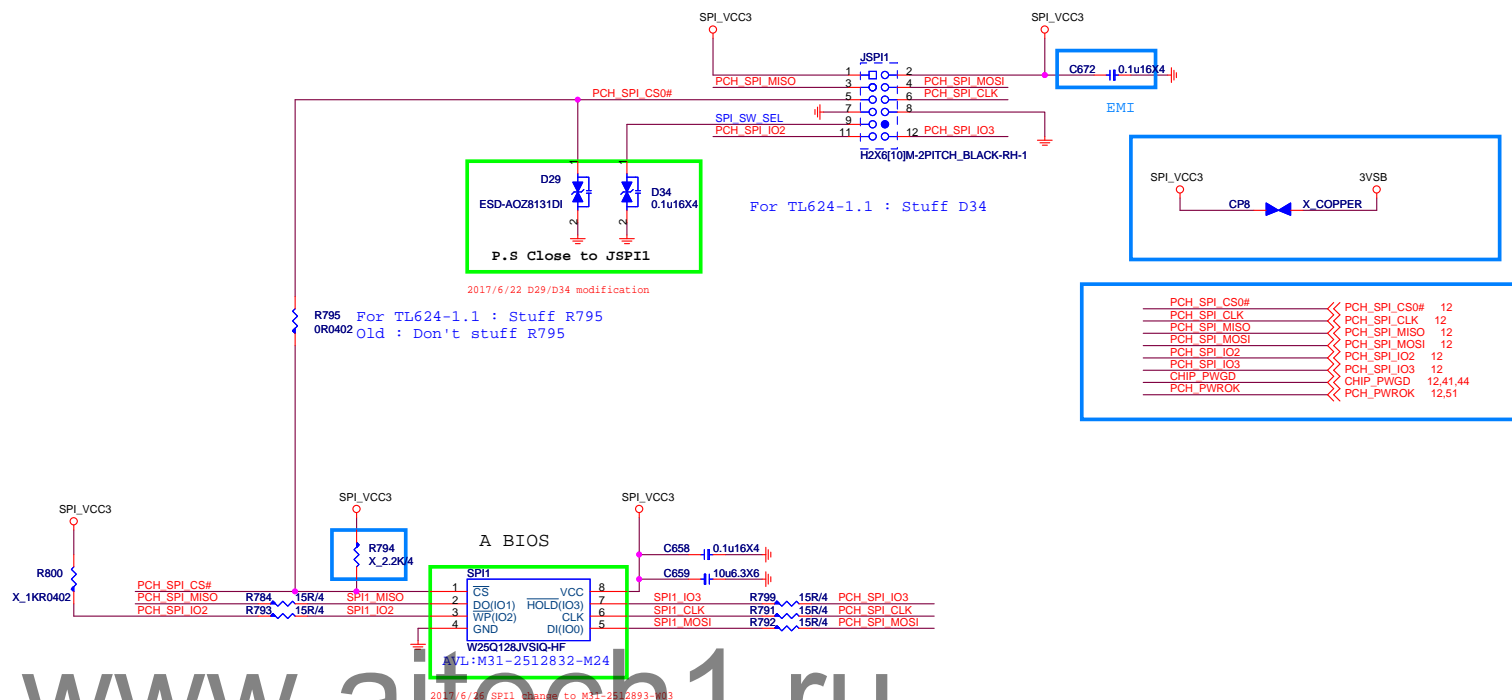
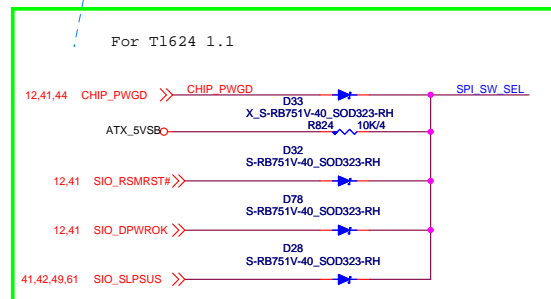
Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default



20160718

Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.



W25Q128JVSIQ-HF
MVL:M31-2512832-M24
2017/6/28 SPI1 change to M31-2512893-M03

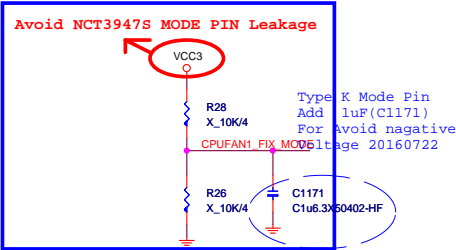
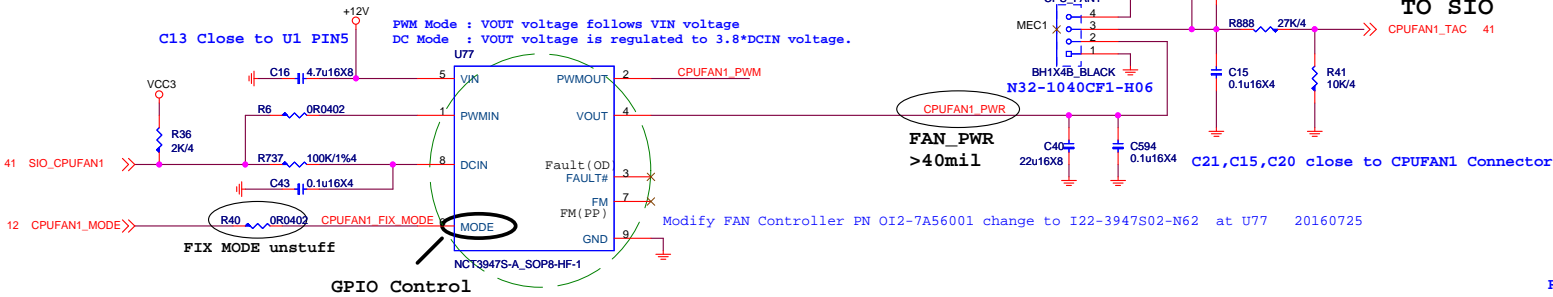


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Size Custom	Document Description BIOS	Rev 10
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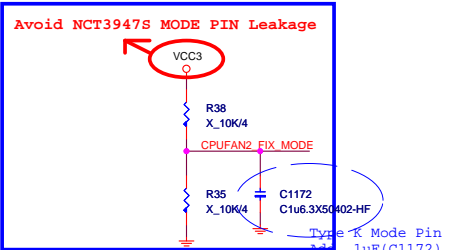
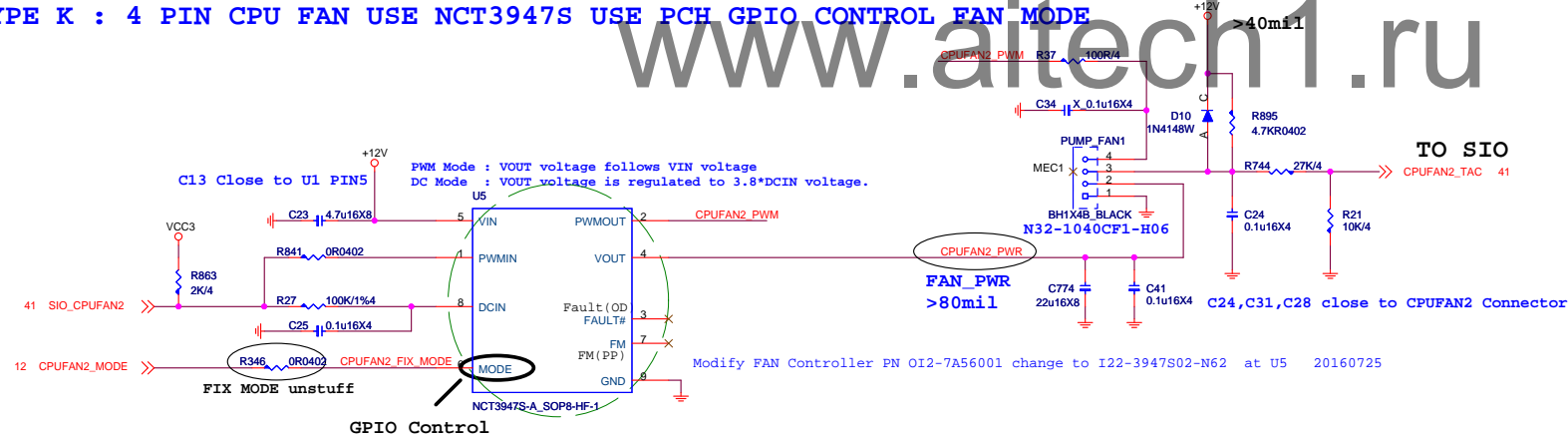
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1.PWM/DC/OCF LED(現在是改成R/G/B3色LED)
- 2.GPIO可以由BIOS切换 PWM/DC MODE
- 3.OCF拉回GPIO給BIOS認
- 4.PWM OR DC FAN拉回GPIO給BIOS認
- 5.FAN轉速加快的時候由SOFTWARE 控制GPIO讓燈的變化



Resever For FIX DC or PWM MODE USE By PM SPEC

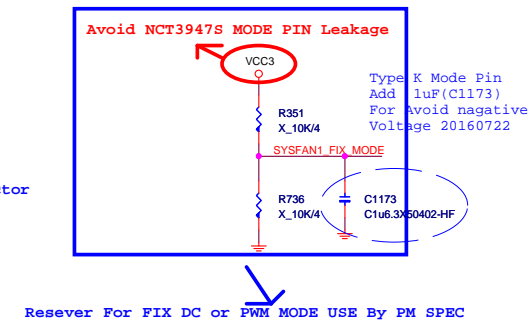
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



Resever For FIX DC or PWM MODE USE By PM SPEC

- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OCF Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

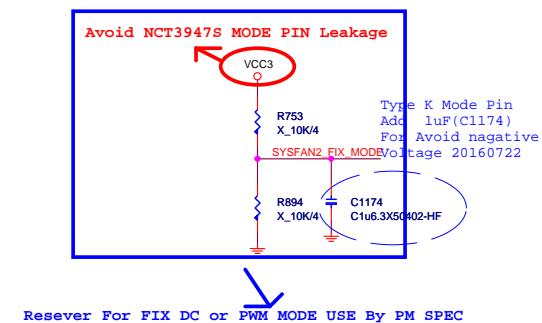
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Internall pull up 1.65V

Default	AUTO MODE	GPI(Floating)
	Internall pull up 1.65V	



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Internall pull up 1.65V

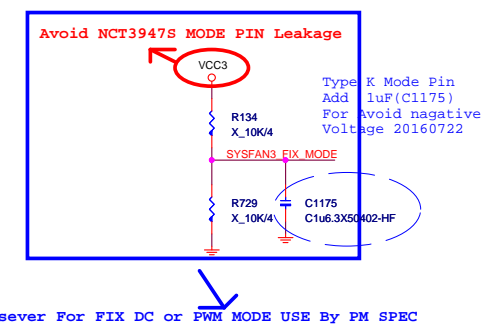
Default	AUTO MODE	GPI(Floating)
	Internall pull up 1.65V	



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Size Custom	Document Description SYSTEM FAN 1/2	Rev 10
Date: Wednesday, August 02, 2017		Sheet 46 of 67

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



Avoid NCT3947S MODE PIN Leakage

VCC3

R352
X_10K/4

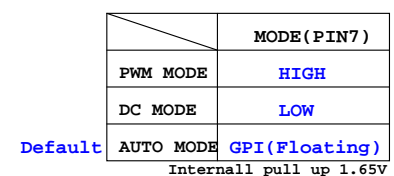
SYSFAN4_FIX MODE

R137
X_10K/4

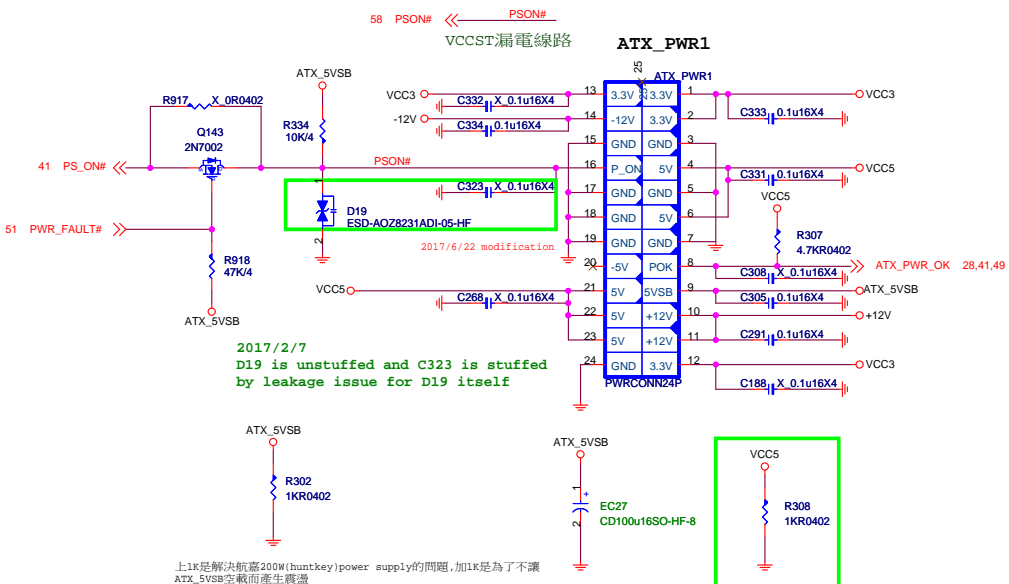
C1176
C1u6.3/50402-HF

Type K Mode Pin
Add 1uF(C1176)
For avoid negative
Voltage 20160722

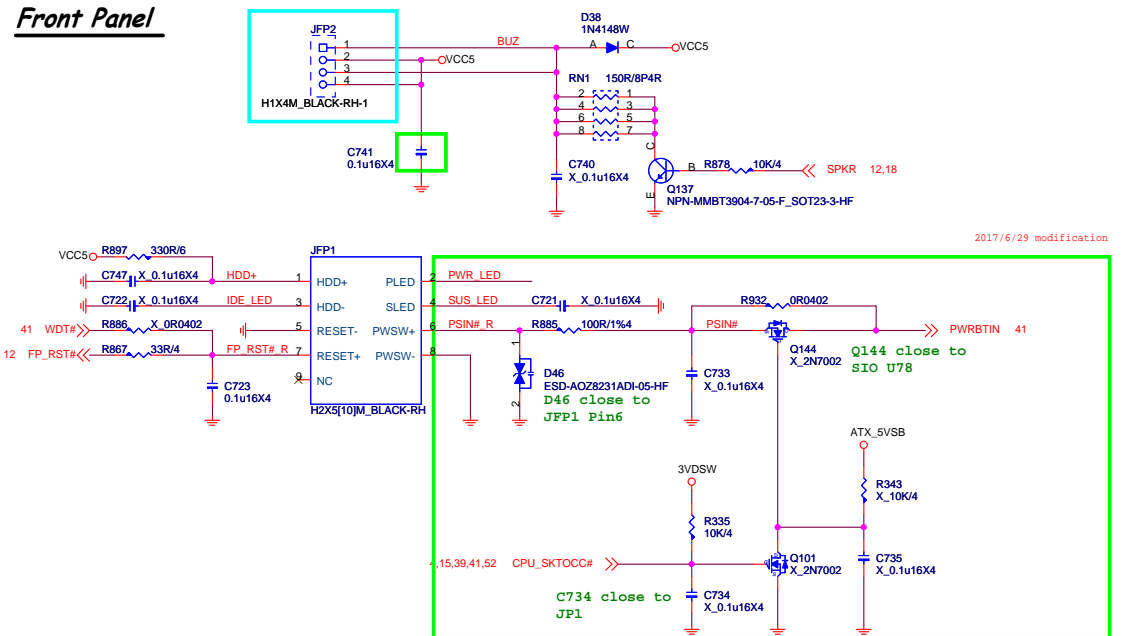
Reserver For FIX DC or PWM MODE USE By PM SPEC



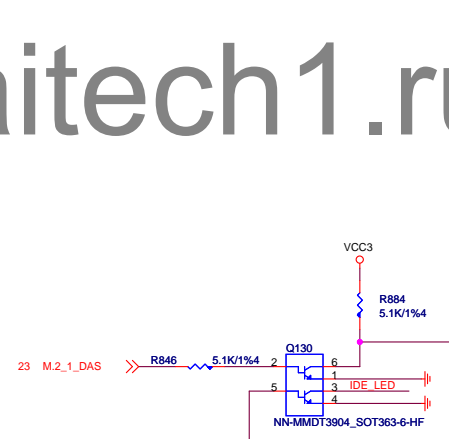
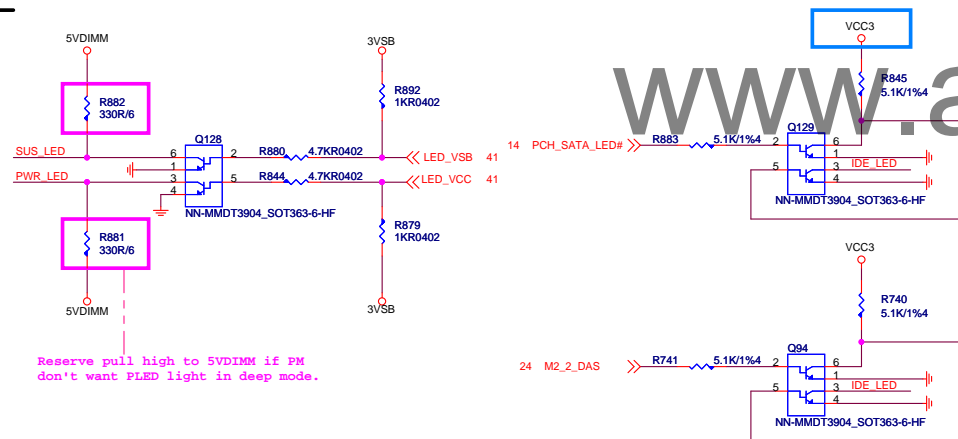
ATX POWER CONNECTOR



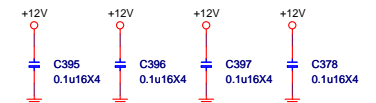
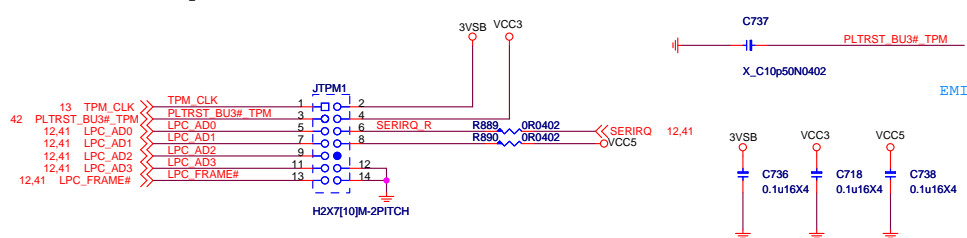
Front Panel



LED



TPM Confirm ESPI TPM card and TPM card pin define
(Not ready)



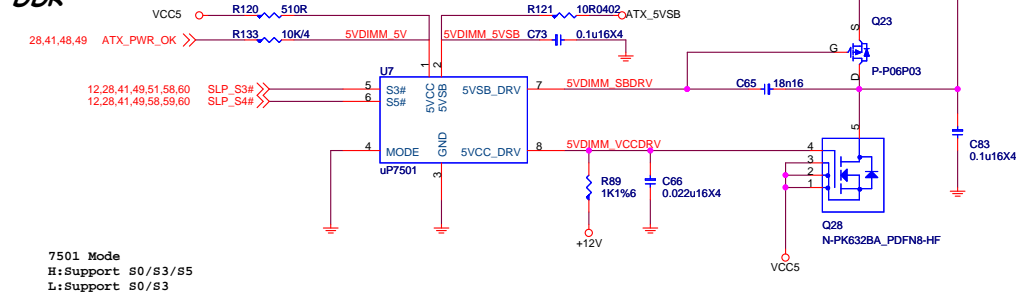
MICRO-STAR INT'L CO.,LTD

MS-7B47

Size Custom	Document Description ATX Power/F_Panel	Rev 10
Date: Wednesday, August 02, 2017		Sheet 48 of 67

5VDIMM FOR DDR

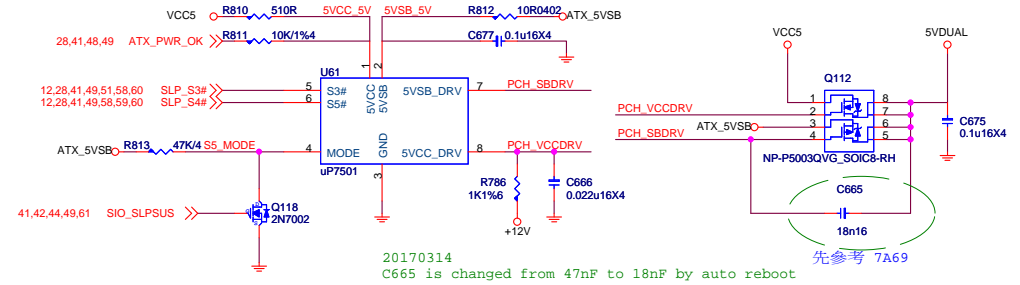
5.45A



5VDUAL

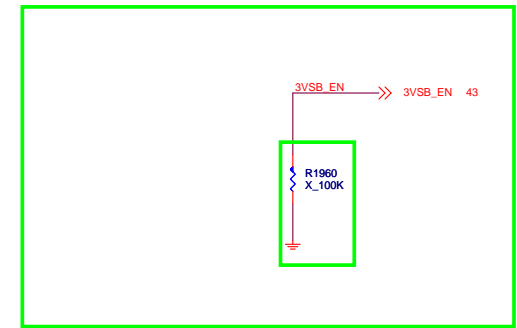
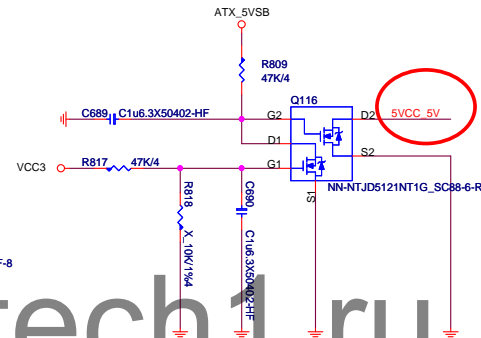
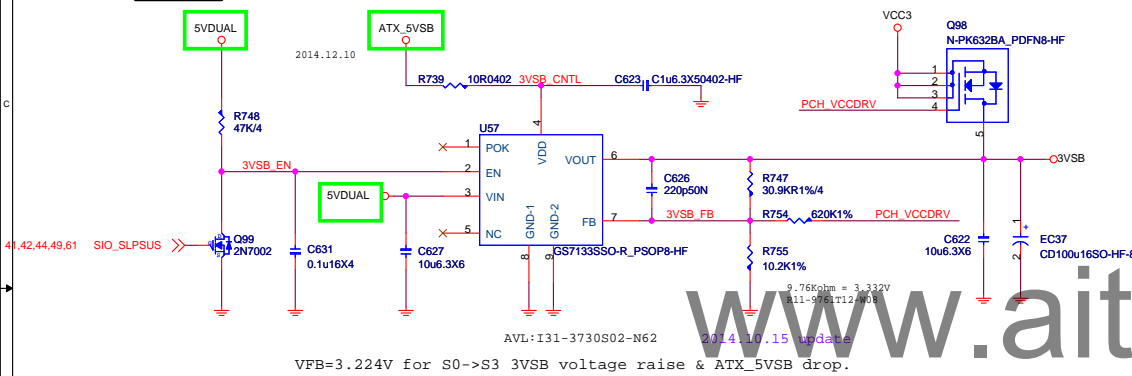
5VDUAL is power source of 1P0SB

PCH:2.95A
3VSB:4.04A
MAX:6.99A



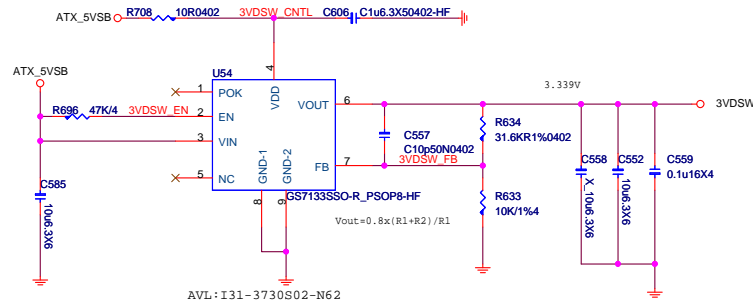
3VSB cost down

4.04A



3VDSW

0.422A



3VDSW EN >>> 3VDSW_EN 43



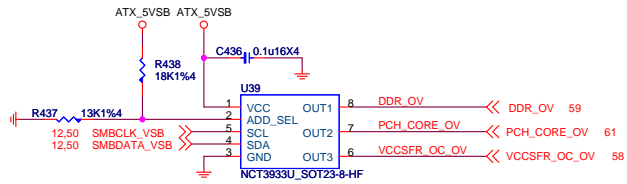
MICRO-STAR INT'L CO.,LTD

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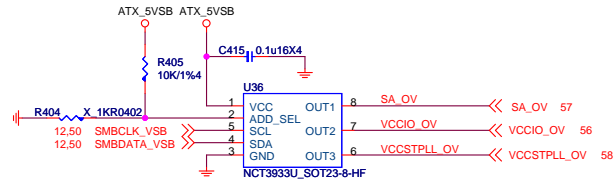
Size	Document Description	Rev
Custom	ACPI UP	10
Date: Wednesday, August 02, 2017	Sheet 49 of 67	

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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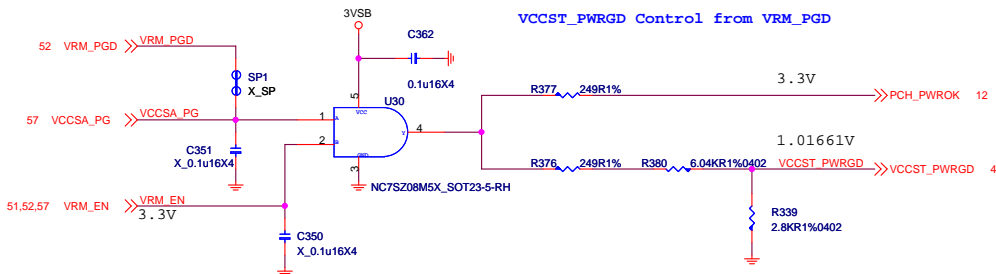
MICRO-STAR INT'L CO.,LTD

MS-7B47

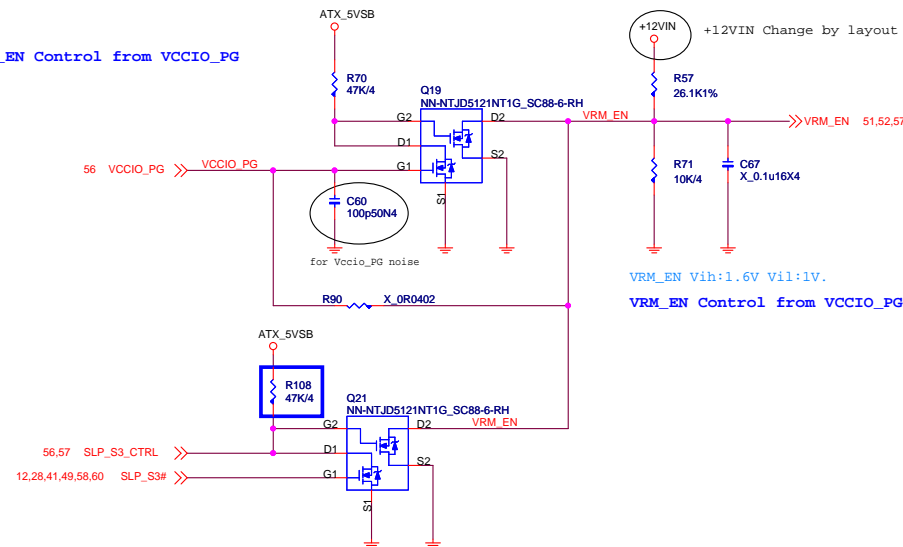
Size Custom	Document Description OV-NCT3933/GPIO-NCT5605	Rev 10
Date: Wednesday, August 02, 2017	Sheet 50 of 67	

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

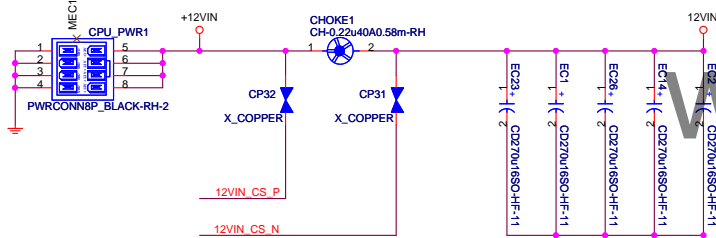
PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PG



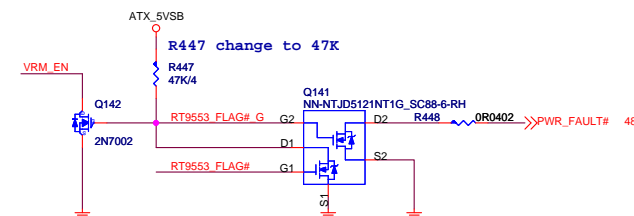
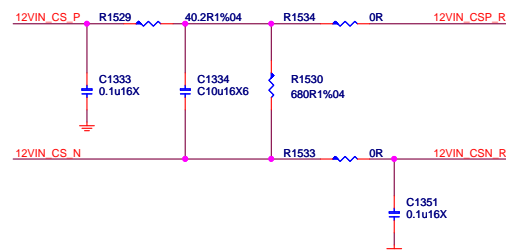
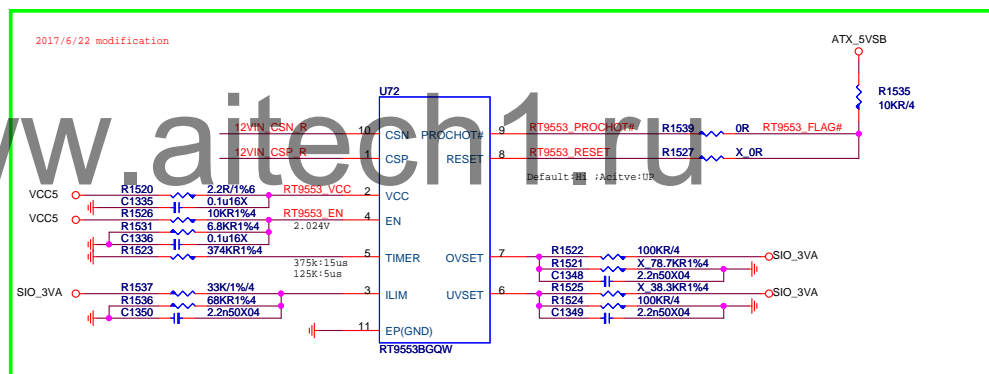
VRM_EN Control from VCCIO_PG



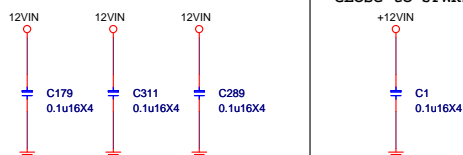
Iripple=30.95A
VCORE 18.101A
VGT 8.457A
VCCSA 4.392A



RT9553B CURRENT SENSE



Close to JPWR2

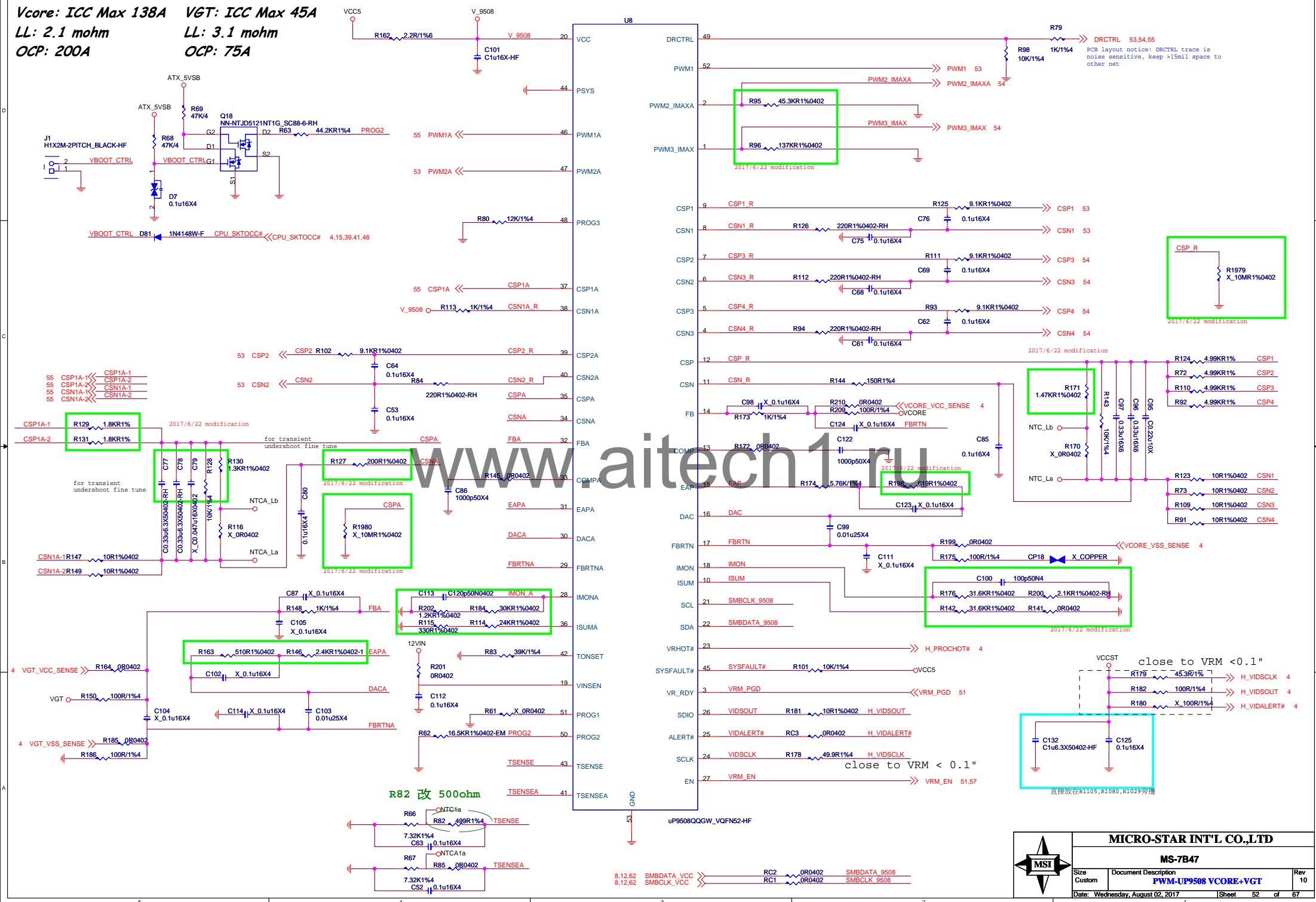


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Size	Document Description	Rev
Custom	Rear I/O P52	10
Date: Wednesday, August 02, 2017	Sheet 51 of 67	

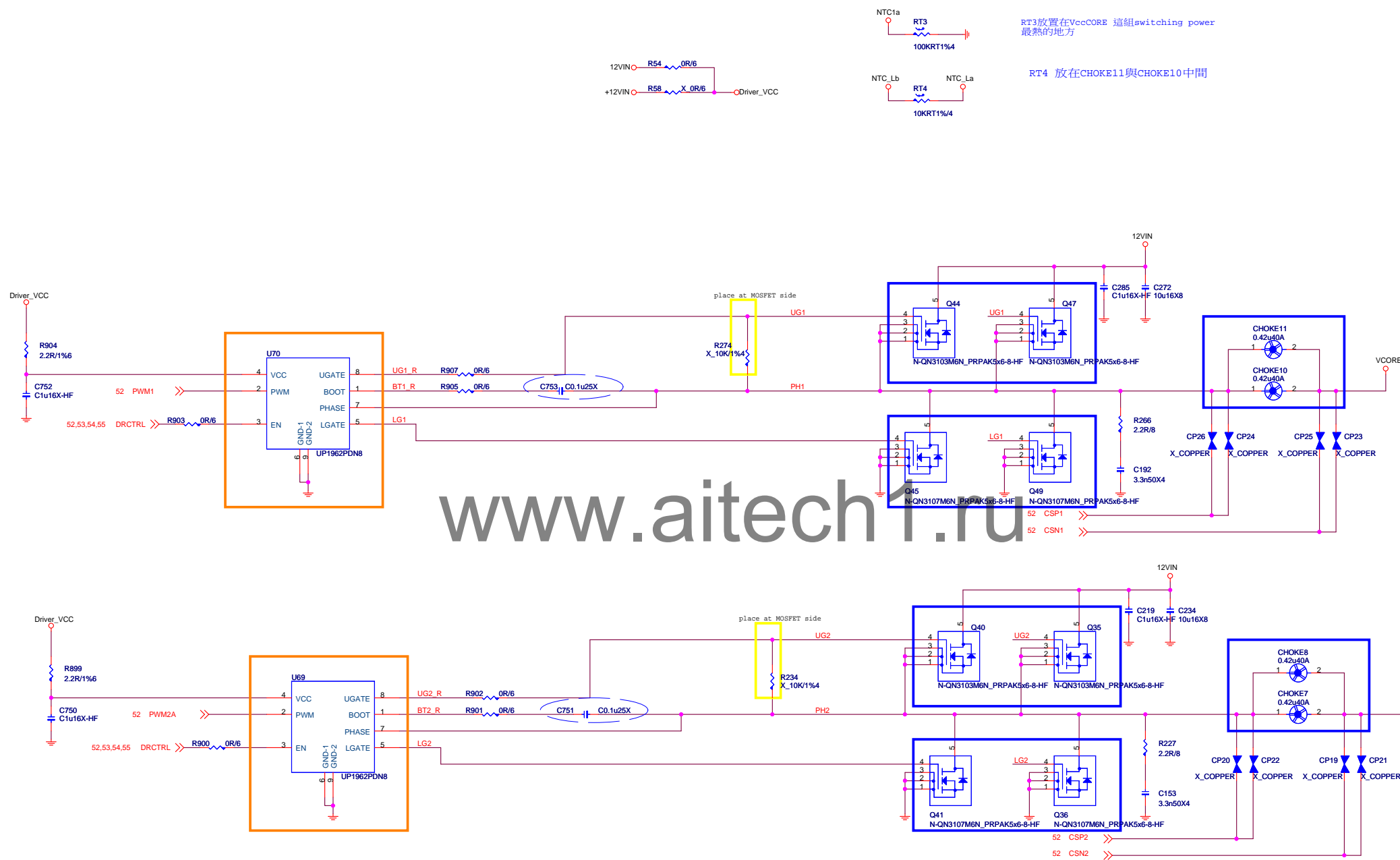
<i>Vcore: ICC Max 138A</i>	<i>VGT: ICC Max 45A</i>
<i>LL: 2.1 mohm</i>	<i>LL: 3.1 mohm</i>
<i>OCP: 200A</i>	<i>OCP: 75A</i>



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Size Custom	Document Description PWM-UP9508 VCORE+VGT	Rev 10
Date: Wednesday, August 02, 2017		Sheet 52 of 67



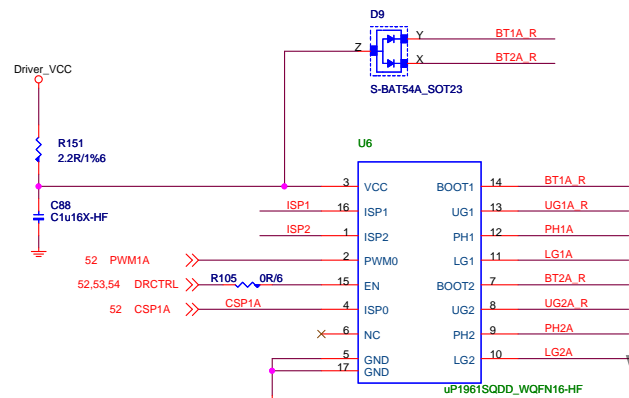
NTC1a
RT3
100KRT1%4

NTC_Lb
RT4
10KRT1%4
NTC_La

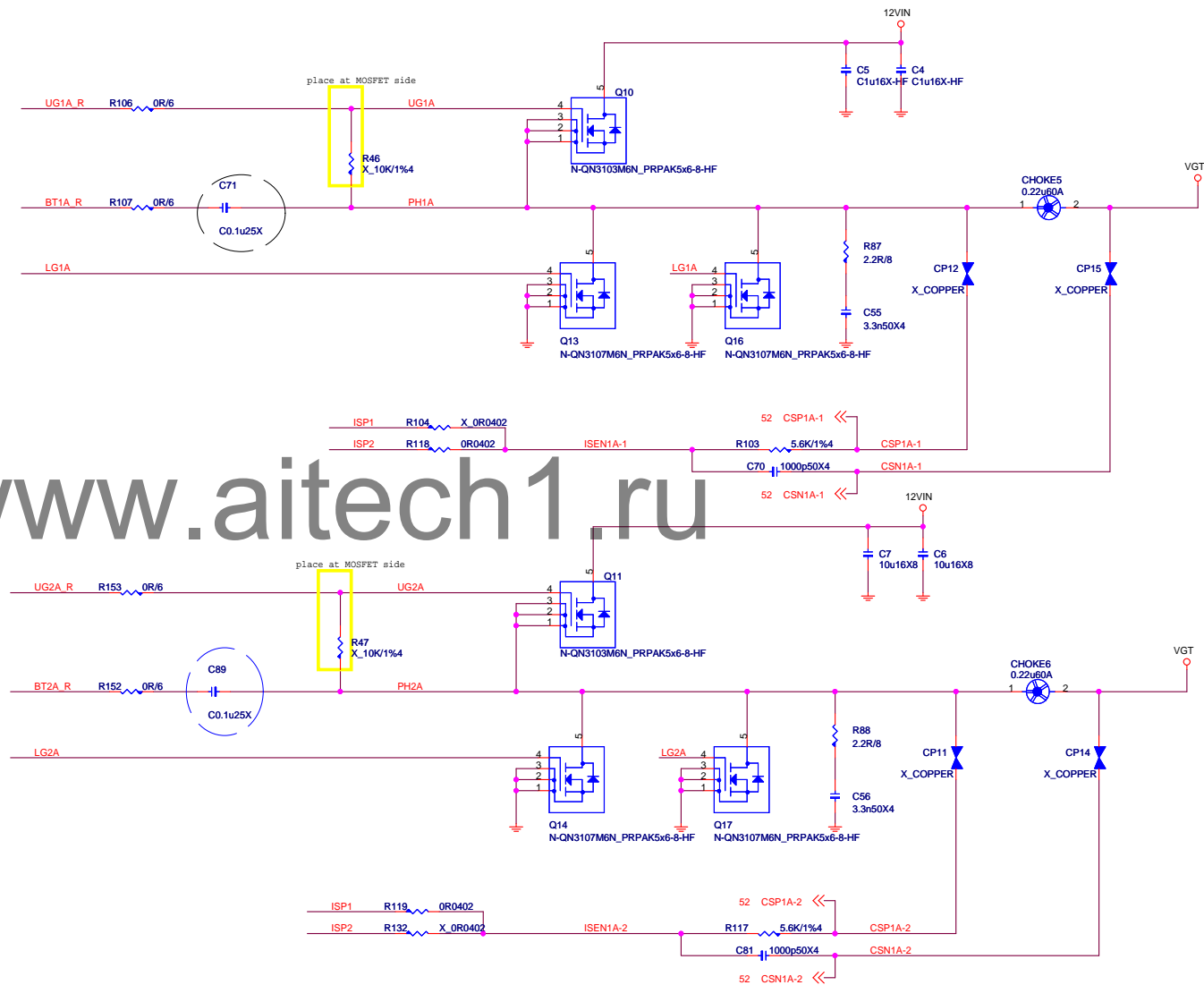
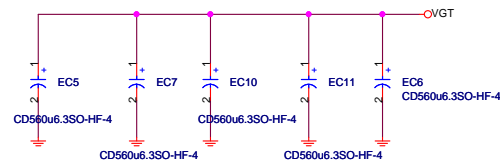
RT3放置在VccCORE 這組switching power 最熱的地方

RT4 放在CHOKE11與CHOKE10中間

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1.0
Z270/H270/B250: I33-1961S0C-U33



RT2 放在 CHOKE5 與 CHOKE6 中間

RT1放置在VccGT 這組switching power 最熱的地方



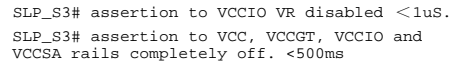
MICRO-STAR INT'L CO.,LTD

MS-7B47

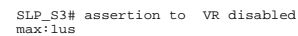
Size	Document Description	Rev
Custom	VGT MOS-PHASE 1-2	10
Date:	Wednesday, August 02, 2017	Sheet 55 of 67

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685



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Rdson(10V)	
D03-4C05N03-O05	: 3.4mohm
D03-632BA0C-N03	: 3.3mohm
D03-3056M00-U47	: 4.2mohm
D03-3107M00-U47	: 2.6mohm



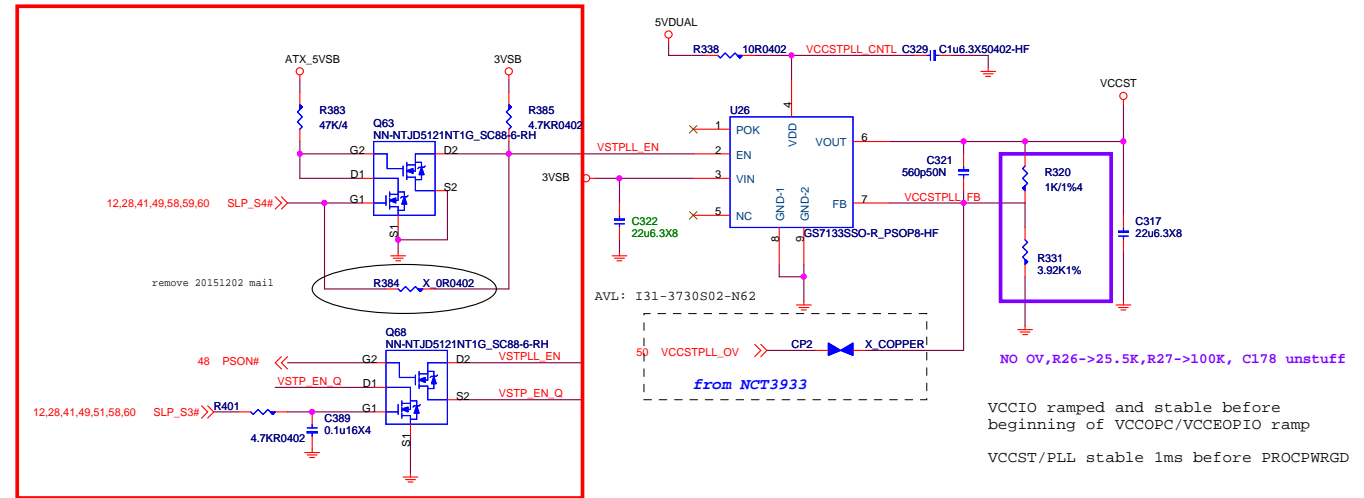
VCCST

VCCST:60mA
VCCPLL:150mA

1.0V; 210mA

For Cost down VCCST&VCCPLL merge

for Gaming3/5, Classic, ECO
and H110

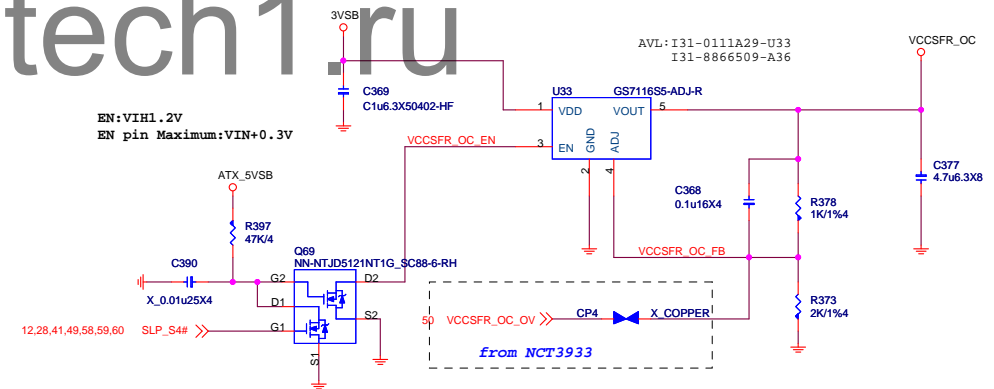


VCCPLL_OC

1.2V; 130mA

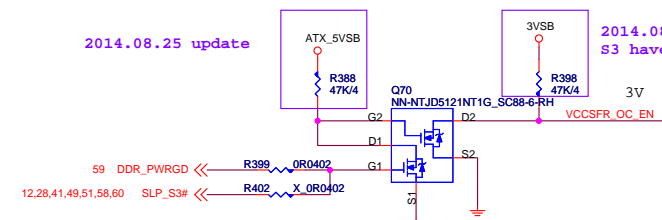
2014.08.21 update

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2014.08.25 update

2014.08.25 update
S3 have power



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MS-7B47			
Size	Document Description		Rev
Custom	CPU PWR ST/PLL		10
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DDR4_1.2V 2.5A+9.5A+1.2A=13.5A
 2.8A FOR CPU
 9.5A FOR 4DIMM
 1.2A FOR DDR VTT

$OCP = 13.2A * 1.5 = 20.25A$
 $Rocs(R95) = OCP * Rdson[Low\ side] / 10uA$
 $= 20.25A * (4.6)mohm / 10uA$
 $= 9.315Kohm$

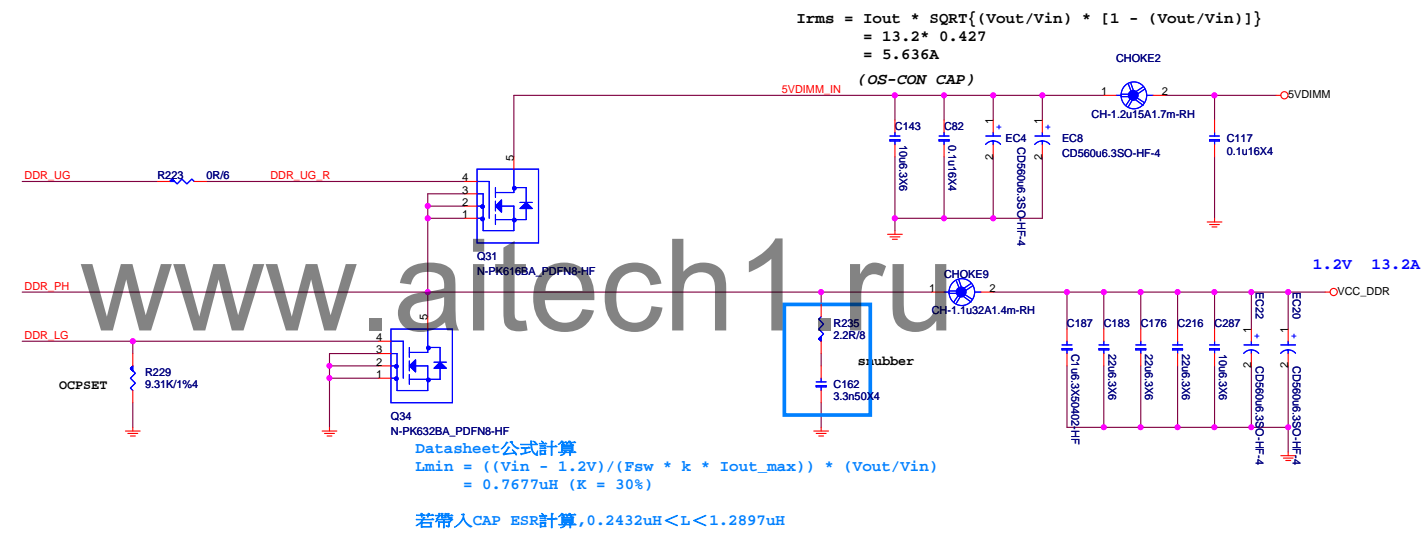
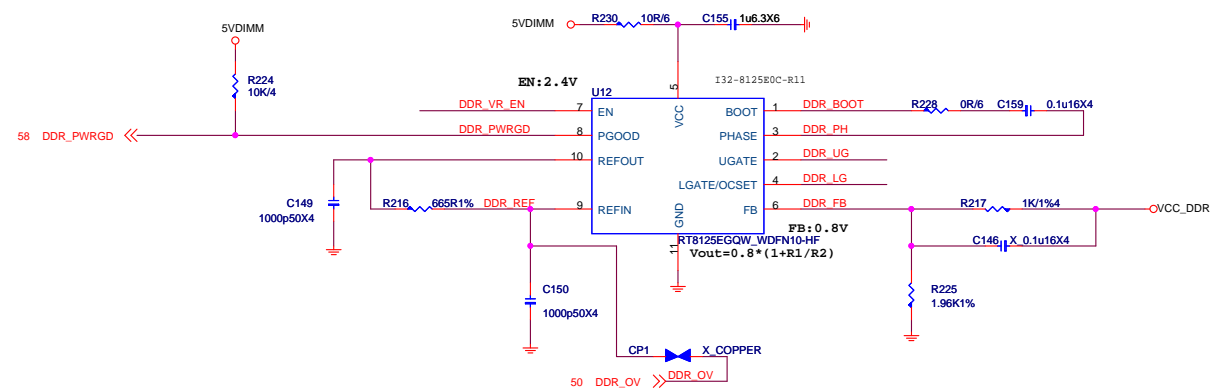
Rocpset:5.1K
 $OCP = Rocset * Rdson[Low\ side] / 10uA$
 $= 9.31K * (4.6)mohm / 10uA$
 $= 20.23A$
 use UBIQ MOS need Check

Rdson(low)4.5V

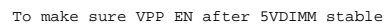
D03-4C05N03-005 : 5 mohm

D03-632BA0C-N03 : 4.6mohm

D03-3056M00-U47 : 6.2mohm

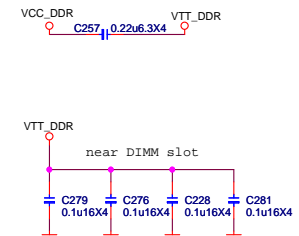
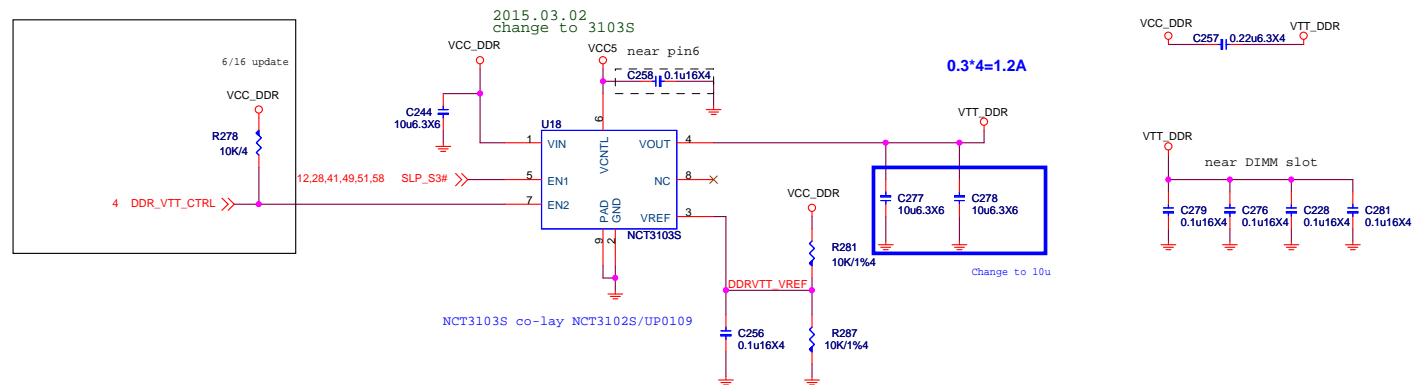


VPP25 Power
2.5V; 2.24A



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2015.03.02
change to 3103S



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Size Custom	Document Description DDR4 Power-VPP25	Rev 10
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PCH_1VSB

1.0V; 11.83A

OCP = 17.745A

Rocset = $1.5 * I_{max} * R_{dson}(low) / I_{ocset}$
 = $1.5 * 11.83 * 4.6mohm / 10uA$
 = 8.16K

Rocs:7.87K,OCP:

D03-4C05N03-005 : 15.74A

D03-632BA0C-N03 : 17.1A

use UBIQ MOS need Check

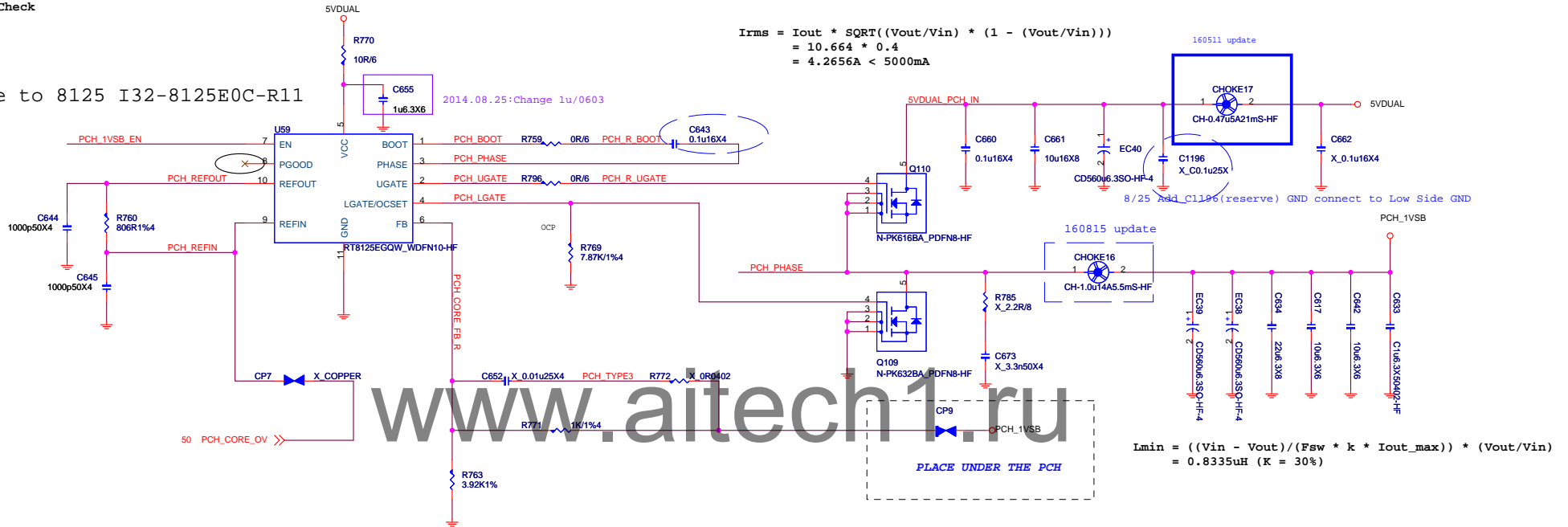
Rdson(low)4.5V

D03-3116M00-U47 : 3.6 mohm

D03-632BA0C-N03 : 4.6mohm

D03-3056M00-U47 : 6.2mohm

1504 change to 8125 I32-8125E0C-R11



$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

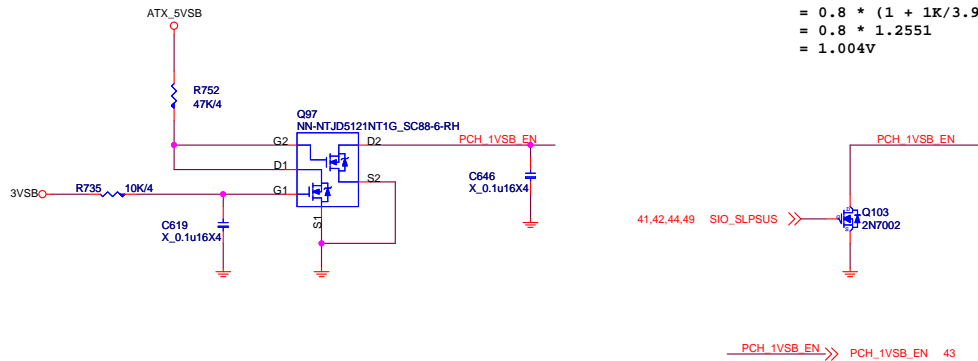
$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$

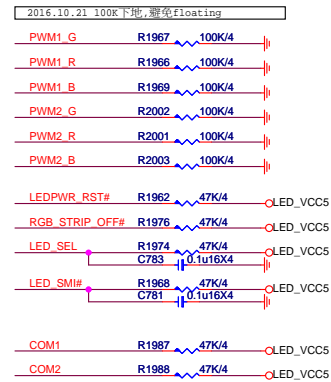
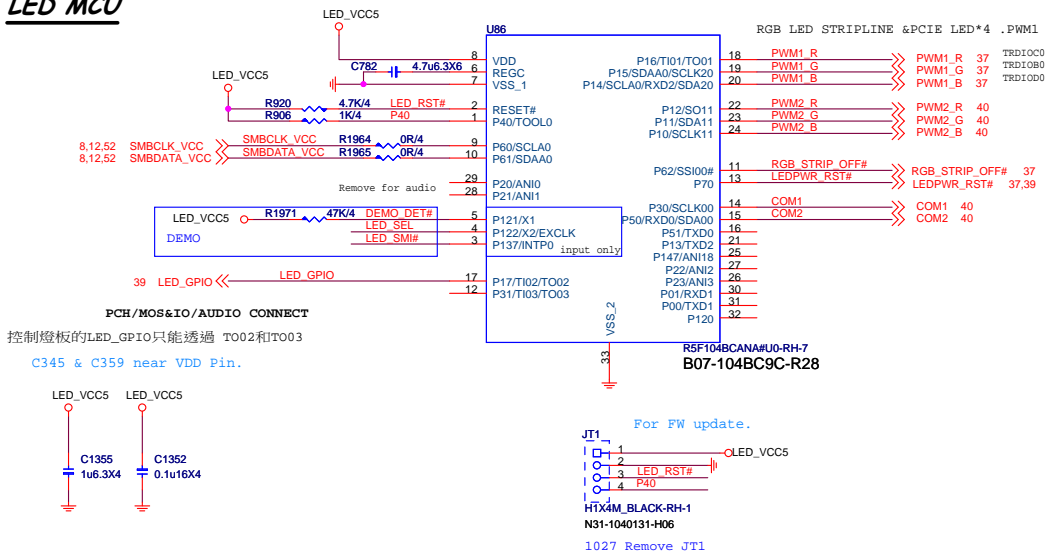


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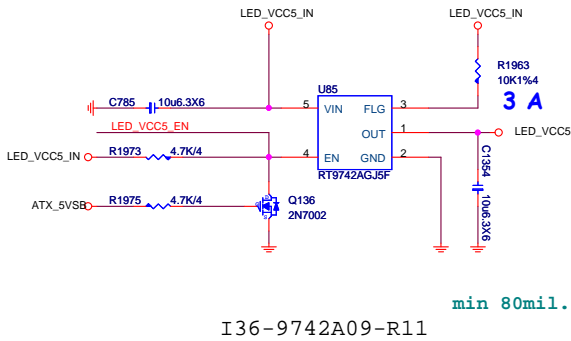
Size	Document Description	Rev
Custom	PCH Core Power-RT8125	10
Date:	Wednesday, August 02, 2017	Sheet 61 of 67

LED MCU

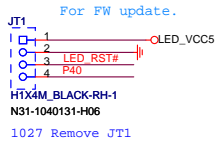


Control	Net Name	PWM USE	Connector
AUDIO Cover	LED_GPIO	No Use	JPIPE_LED1
PCH	LED_GPIO_01	No Use	JPIPE_LED2
MOS/IO cover	LED_GPIO_02	No Use	JPIPE_LED3
LED STRIPLINE	RGB_STRIP_OFF#	PWM1	JLED1
Board Side LED	COM1-8	PWM2	RGB LED
PCIE Side LED	COM1-4	PWM1	RGB LED

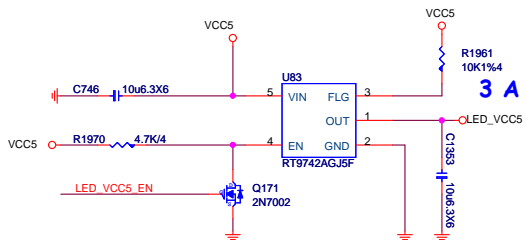
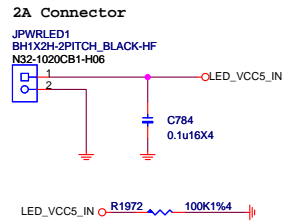
EXTERNAL POWER INPUT



LED Demo Button



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Size Custom	Document Description LED MCU	Rev 11
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